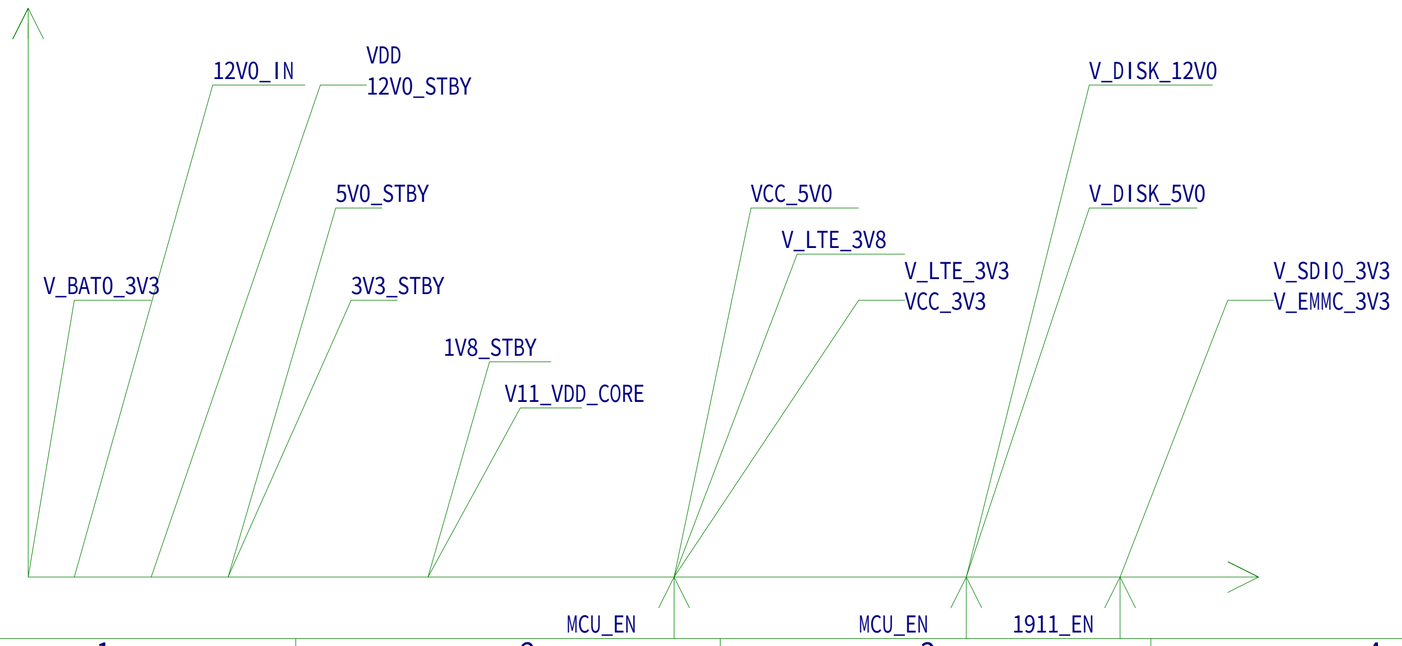
Atlas 200I A2 底板电路参考设计

Department：Ascend Computing Hardware Program

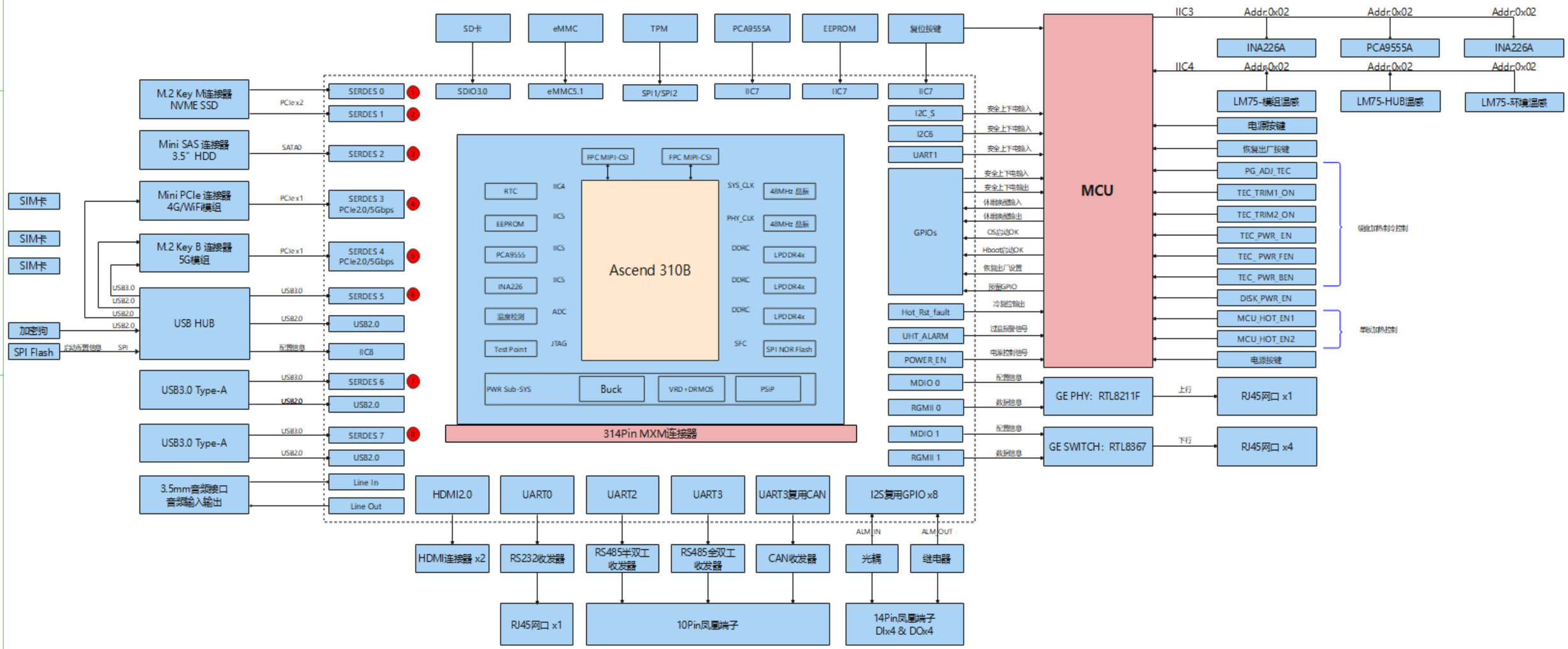
Power Tree

V_12V0_IN
VDD 12V/3A
模组
V_STBY_12V0 4.9A
DC-DC
V_STBY_5V
SW
DISK_12V_EN
V_VCC_DISK_5V0 700mA
3.5 HDD
SW
MCU_EN
V_USB_5V0 1A
USB HUB
HDMI_TX_5V 100mA
HDMI
V_STBY_5V 96mA
DC-DC
V_STBY_1V8
SW
1911_EN
V_VCC_1V8_EMMC 180mA
eMMC
61mA
GE SW
DC-DC
V_STBY_3V3
SW
MCU_EN
DC-DC
V_LTE_3V3 800mA
4G Module
SW
MCU_EN
DC-DC
V_LTE_3V8 853mA
5G Module
SW
MCU_EN
V_HOT_12V 3A
加热电阻
SW
MCU_EN
V_VCC_DISK_12V0 550mA
3.5 HDD
DC-DC
V_ADJ_TEC 2.5V/4A
TEC Module
DC-DC
V11_VDD_CORE 805mA
GE SW
V_STBY_3V3 650mA
GE SW
V_STBY_3V3 230mA
PHY
V_STBY_3V3 200mA
MCU
V_STBY_3V3
SW
1911_EN
V_VCC_3V3_EMMC 200mA
eMMC
V_STBY_3V3
SW
1911_EN
V_SDCARD_V33 200mA
Micro SD
V_STBY_3V3
SW
MCU_EN
V_VCC_3V3 365mA
USB HUB
1.2A
NVME SSD

Power Sequence



Block Diagram



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I2C Block Diagram

模组
314Pin MXM

Master I2C7
Master I2C8
Master I2C6
Slave I2CS

Addr:FW TBD
USB HUB

Addr:FW TBD
4G

Addr:0xA0
电子标签
EEPROM

Addr:0x42
ID
TPM

Addr:0x40
BOM ID
PCA9555

I2C1 Slave
MCU
I2C2 Master
Master I2C3
Master I2C0
Master I2C4
Master I2C7

Addr:0x96
Temp
ADT75

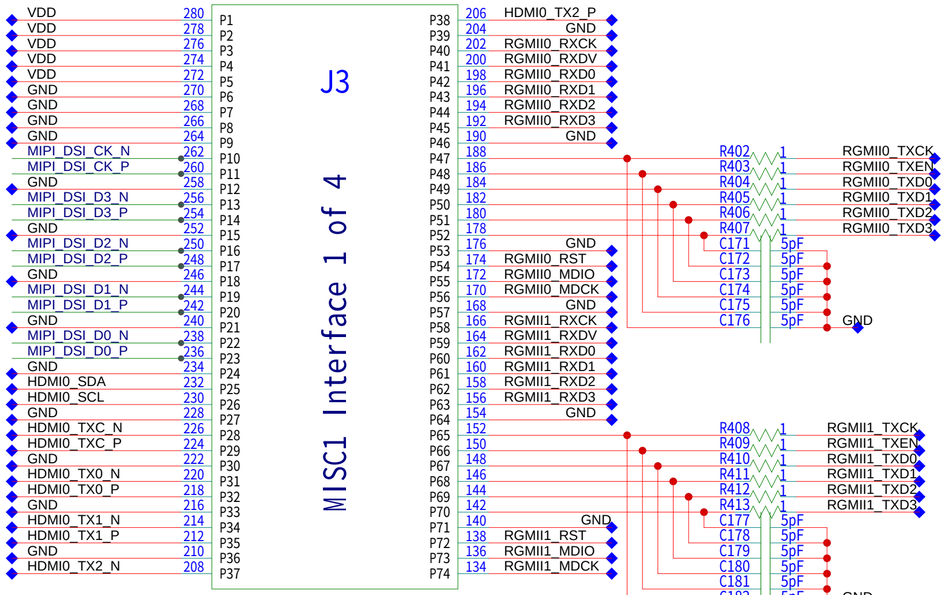
Addr:0x94
Temp
ADT75

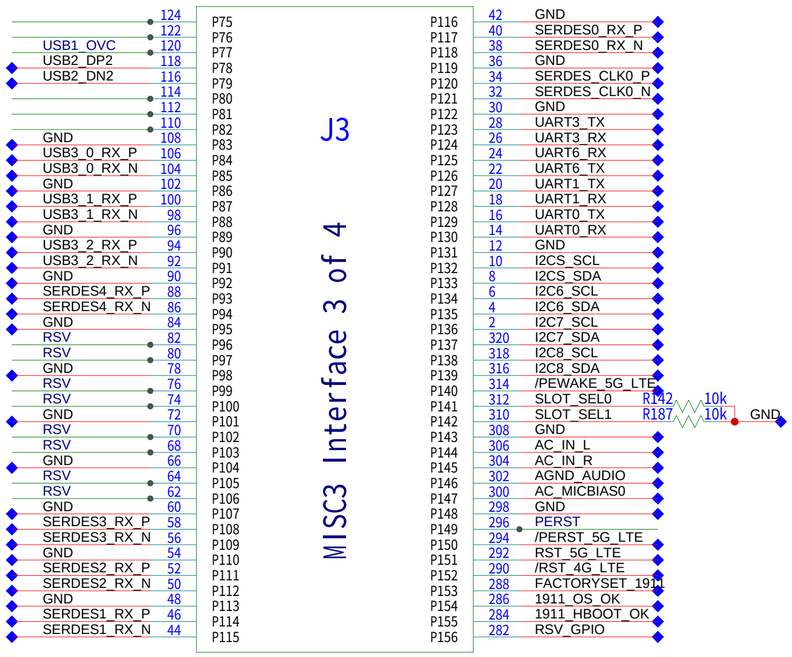
Addr:0x92
Temp
ADT75

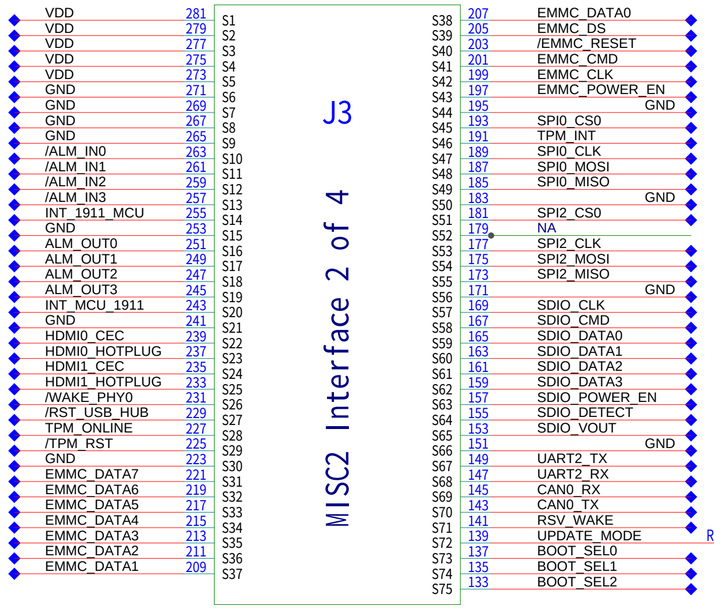
Addr:0x80
PWR DET
TPA626

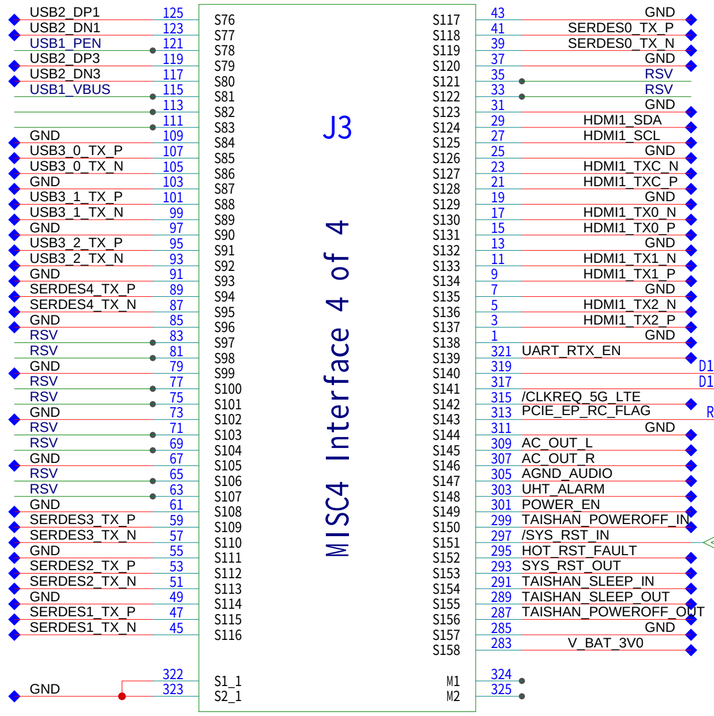
Addr:0x42
TEC
PCA9555

Addr:TBD
PLL
100M_CLK

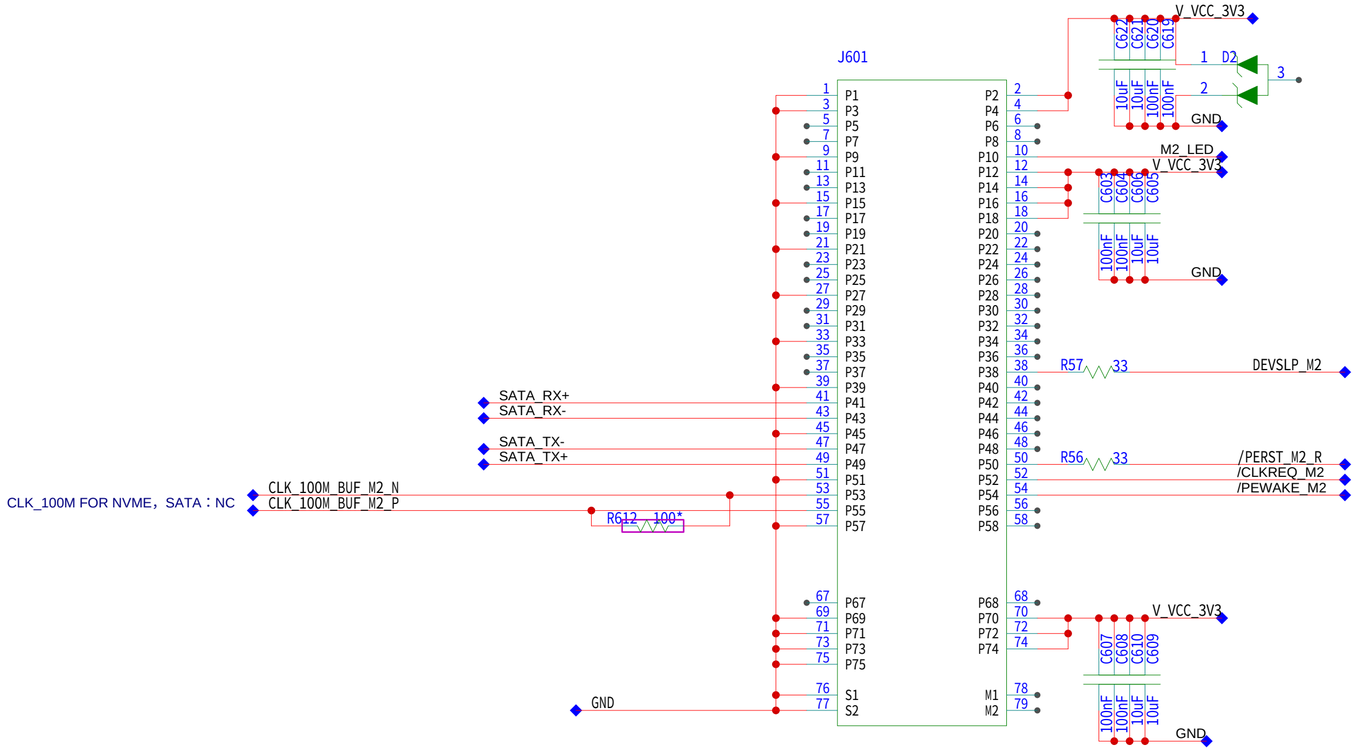

J3
MISC1 Interface 1 of 4
VDD 280
VDD 278
VDD 276
VDD 274
VDD 272
GND 270
GND 268
GND 266
GND 264
MIPI_DSI_CK_N 262
MIPI_DSI_CK_P 260
GND 258
MIPI_DSI_D3_N 256
MIPI_DSI_D3_P 254
GND 252
MIPI_DSI_D2_N 250
MIPI_DSI_D2_P 248
GND 246
MIPI_DSI_D1_N 244
MIPI_DSI_D1_P 242
GND 240
MIPI_DSI_D0_N 238
MIPI_DSI_D0_P 236
GND 234
HDMI0_SDA 232
HDMI0_SCL 230
GND 228
HDMI0_TXC_N 226
HDMI0_TXC_P 224
GND 222
HDMI0_TX0_N 220
HDMI0_TX0_P 218
GND 216
HDMI0_TX1_N 214
HDMI0_TX1_P 212
GND 210
HDMI0_TX2_N 208
P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 P16 P17 P18 P19 P20 P21 P22 P23 P24 P25 P26 P27 P28 P29 P30 P31 P32 P33 P34 P35 P36 P37
P38 206 HDMI0_TX2_P
P39 204 GND
P40 202 RGMII0_RXCK
P41 200 RGMII0_RXDV
P42 198 RGMII0_RXD0
P43 196 RGMII0_RXD1
P44 194 RGMII0_RXD2
P45 192 RGMII0_RXD3
P46 190 GND
P47 188
P48 186
P49 184
P50 182
P51 180
P52 178
P53 176 GND
P54 174 RGMII0_RST
P55 172 RGMII0_MDIO
P56 170 RGMII0_MDCK
P57 168 GND
P58 166 RGMII1_RXCK
P59 164 RGMII1_RXDV
P60 162 RGMII1_RXD0
P61 160 RGMII1_RXD1
P62 158 RGMII1_RXD2
P63 156 RGMII1_RXD3
P64 154 GND
P65 152
P66 150
P67 148
P68 146
P69 144
P70 142
P71 140 GND
P72 138 RGMII1_MDIO
P73 136 RGMII1_MDCK
P74 134
R402 1 RGMII0_TXCK
R403 1 RGMII0_TXEN
R404 1 RGMII0_TXD0
R405 1 RGMII0_TXD1
R406 1 RGMII0_TXD2
R407 1 RGMII0_TXD3
C171 5pF
C172 5pF
C173 5pF
C174 5pF
C175 5pF
C176 5pF GND
R408 1 RGMII1_TXCK
R409 1 RGMII1_TXEN
R410 1 RGMII1_TXD0
R411 1 RGMII1_TXD1
R412 1 RGMII1_TXD2
R413 1 RGMII1_TXD3
C177 5pF
C178 5pF
C179 5pF
C180 5pF
C181 5pF
C182 5pF GND

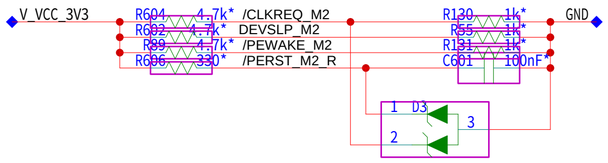

J3
MISC3 Interface 3 of 4
124
122
USB1_OVC 120
USB2_DP2 118
USB2_DN2 116
114
112
110
GND 108
USB3_0_RX_P 106
USB3_0_RX_N 104
GND 102
USB3_1_RX_P 100
USB3_1_RX_N 98
GND 96
USB3_2_RX_P 94
USB3_2_RX_N 92
GND 90
SERDES4_RX_P 88
SERDES4_RX_N 86
GND 84
RSV 82
RSV 80
GND 78
RSV 76
RSV 74
GND 72
RSV 70
RSV 68
GND 66
RSV 64
RSV 62
GND 60
SERDES3_RX_P 58
SERDES3_RX_N 56
GND 54
SERDES2_RX_P 52
SERDES2_RX_N 50
GND 48
SERDES1_RX_P 46
SERDES1_RX_N 44
P75 P76 P77 P78 P79 P80 P81 P82 P83 P84 P85 P86 P87 P88 P89 P90 P91 P92 P93 P94 P95 P96 P97 P98 P99 P100 P101 P102 P103 P104 P105 P106 P107 P108 P109 P110 P111 P112 P113 P114 P115
P116 42 GND
P117 40 SERDES0_RX_P
P118 38 SERDES0_RX_N
P119 36 GND
P120 34 SERDES_CLK0_P
P121 32 SERDES_CLK0_N
P122 30 GND
P123 28 UART3_TX
P124 26 UART3_RX
P125 24 UART6_RX
P126 22 UART6_TX
P127 20 UART1_TX
P128 18 UART1_RX
P129 16 UART0_TX
P130 14 UART0_RX
P131 12 GND
P132 10 I2CS_SCL
P133 8 I2CS_SDA
P134 6 I2C6_SCL
P135 4 I2C6_SDA
P136 2 I2C7_SCL
P137 320 I2C7_SDA
P138 318 I2C8_SCL
P139 316 I2C8_SDA
P140 314 /PEWAKE_5G_LTE
P141 312 SLOT_SEL0 R142 10k
P142 310 SLOT_SEL1 R187 10k GND
P143 308 GND
P144 306 AC_IN_L
P145 304 AC_IN_R
P146 302 AGND_AUDIO
P147 300 AC_MICBIAS0
P148 298 GND
P149 296 PERST
P150 294 /PERST_5G_LTE
P151 292 RST_5G_LTE
P152 290 /RST_4G_LTE
P153 288 FACTORYSET_1911
P154 286 1911_OS_OK
P155 284 1911_HBOOT_OK
P156 282 RSV_GPIO

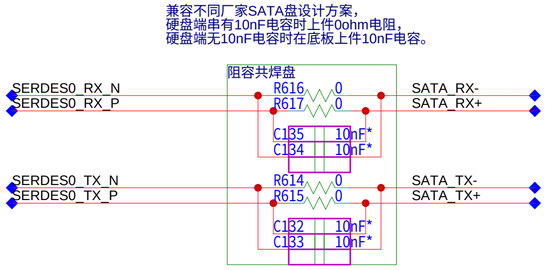

J3
MISC2 Interface 2 of 4
VDD 281
VDD 279
VDD 277
VDD 275
VDD 273
GND 271
GND 269
GND 267
GND 265
/ALM_IN0 263
/ALM_IN1 261
/ALM_IN2 259
/ALM_IN3 257
INT_1911_MCU 255
GND 253
ALM_OUT0 251
ALM_OUT1 249
ALM_OUT2 247
ALM_OUT3 245
INT_MCU_1911 243
GND 241
HDMI0_CEC 239
HDMI0_HOTPLUG 237
HDMI1_CEC 235
HDMI1_HOTPLUG 233
/WAKE_PHY0 231
/RST_USB_HUB 229
TPM_ONLINE 227
/TPM_RST 225
GND 223
EMMC_DATA7 221
EMMC_DATA6 219
EMMC_DATA5 217
EMMC_DATA4 215
EMMC_DATA3 213
EMMC_DATA2 211
EMMC_DATA1 209
S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16 S17 S18 S19 S20 S21 S22 S23 S24 S25 S26 S27 S28 S29 S30 S31 S32 S33 S34 S35 S36 S37
S38 207 EMMC_DATA0
S39 205 EMMC_DS
S40 203 /EMMC_RESET
S41 201 EMMC_CMD
S42 199 EMMC_CLK
S43 197 EMMC_POWER_EN
S44 195 GND
S45 193 SPI0_CS0
S46 191 TPM_INT
S47 189 SPI0_CLK
S48 187 SPI0_MOSI
S49 185 SPI0_MISO
S50 183 GND
S51 181 SPI2_CS0
S52 179 NA
S53 177 SPI2_CLK
S54 175 SPI2_MOSI
S55 173 SPI2_MISO
S56 171 GND
S57 169 SDIO_CLK
S58 167 SDIO_CMD
S59 165 SDIO_DATA0
S60 163 SDIO_DATA1
S61 161 SDIO_DATA2
S62 159 SDIO_DATA3
S63 157 SDIO_POWER_EN
S64 155 SDIO_DETECT
S65 153 SDIO_VOUT
S66 151 GND
S67 149 UART2_TX
S68 147 UART2_RX
S69 145 CAN0_RX
S70 143 CAN0_TX
S71 141 RSV_WAKE
S72 139 UPDATE_MODE R83 1k* GND
S73 137 BOOT_SEL0
S74 135 BOOT_SEL1
S75 133 BOOT_SEL2

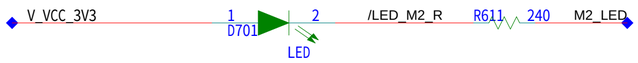

J3
MISC4 Interface 4 of 4
USB2_DP1 125
USB2_DN1 123
USB1_PEN 121
USB2_DP3 119
USB2_DN3 117
USB1_VBUS 115
113
111
GND 109
USB3_0_TX_P 107
USB3_0_TX_N 105
GND 103
USB3_1_TX_P 101
USB3_1_TX_N 99
GND 97
USB3_2_TX_P 95
USB3_2_TX_N 93
GND 91
SERDES4_TX_P 89
SERDES4_TX_N 87
GND 85
RSV 83
RSV 81
GND 79
RSV 77
RSV 75
GND 73
RSV 71
RSV 69
GND 67
RSV 65
RSV 63
GND 61
SERDES3_TX_P 59
SERDES3_TX_N 57
GND 55
SERDES2_TX_P 53
SERDES2_TX_N 51
GND 49
SERDES1_TX_P 47
SERDES1_TX_N 45
322
GND 323
S1_1
S2_1
S76 S77 S78 S79 S80 S81 S82 S83 S84 S85 S86 S87 S88 S89 S90 S91 S92 S93 S94 S95 S96 S97 S98 S99 S100 S101 S102 S103 S104 S105 S106 S107 S108 S109 S110 S111 S112 S113 S114 S115 S116
S117 43 GND
S118 41 SERDES0_TX_P
S119 39 SERDES0_TX_N
S120 37 GND
S121 35 RSV
S122 33 RSV
S123 31 GND
S124 29 HDMI1_SDA
S125 27 HDMI1_SCL
S126 25 GND
S127 23 HDMI1_TXC_N
S128 21 HDMI1_TXC_P
S129 19 GND
S130 17 HDMI1_TX0_N
S131 15 HDMI1_TX0_P
S132 13 GND
S133 11 HDMI1_TX1_N
S134 9 HDMI1_TX1_P
S135 7 GND
S136 5 HDMI1_TX2_N
S137 3 HDMI1_TX2_P
S138 1 GND
S139 321 UART_RTX_EN
S140 319 D18 2 D_A 1
S141 317 D19 2 1 SATA_LED
S142 315 /CLKREQ_5G_LTE D_A
S143 313 PCIE_EP_RC_FLAG R208 1k GND
S144 311 GND
S145 309 AC_OUT_L
S146 307 AC_OUT_R
S147 305 AGND_AUDIO
S148 303 UHT_ALARM
S149 301 POWER_EN
S150 299 TAISHAN_POWEROFF_IN
S151 297 /SYS_RST_IN
S152 295 HOT_RST_FAULT
S153 293 SYS_RST_OUT
S154 291 TAISHAN_SLEEP_IN
S155 289 TAISHAN_SLEEP_OUT
S156 287 TAISHAN_POWEROFF_OUT
S157 285 GND
S158 283 V_BAT_3V0
M1 324
M2 325
整板全局复位
模组挂死，通知MCU复位模组

M.2 SATA SSD









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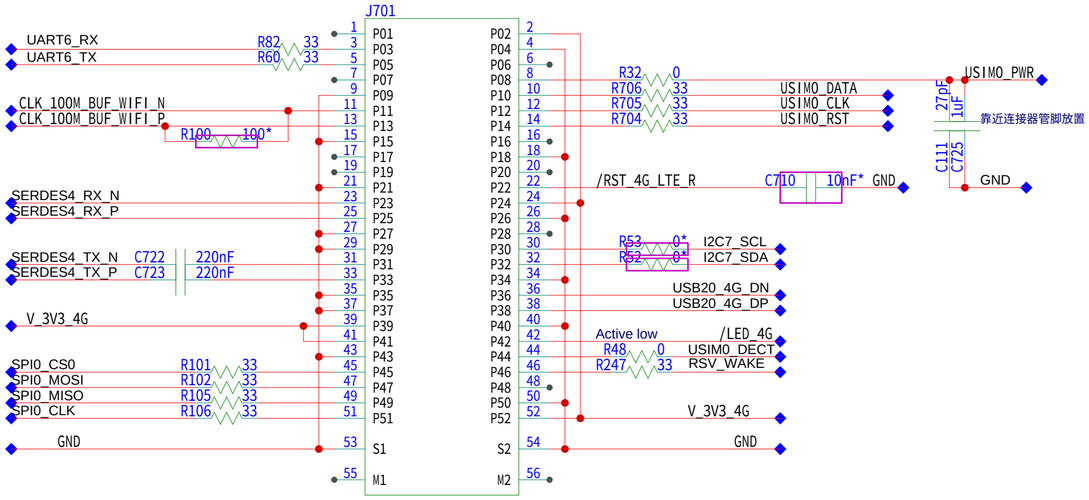
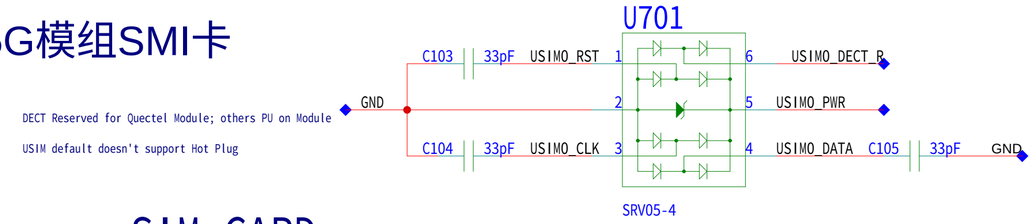
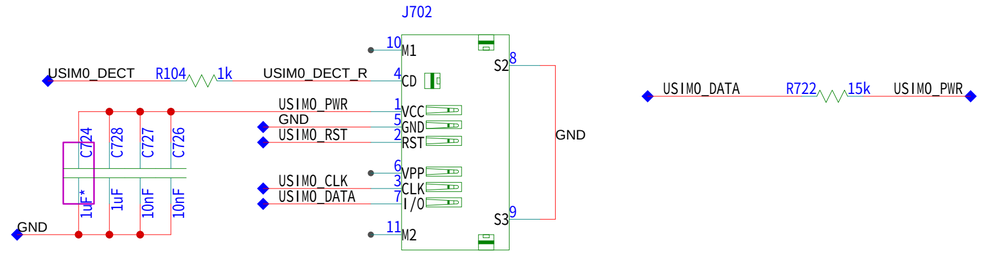
Mini WiFi/4G



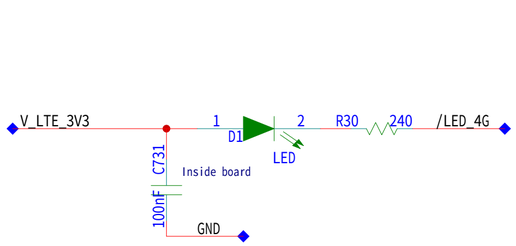
4/5G模组SMI卡

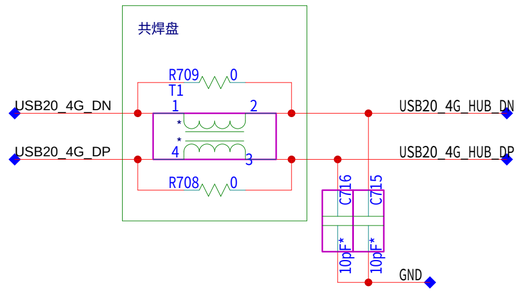


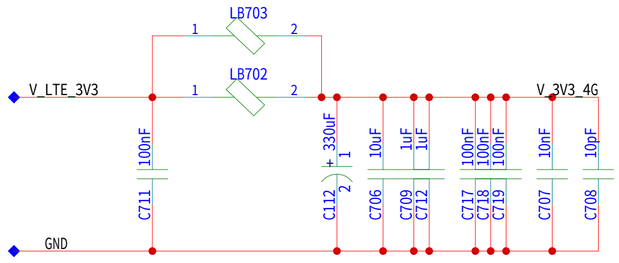
SIM CARD



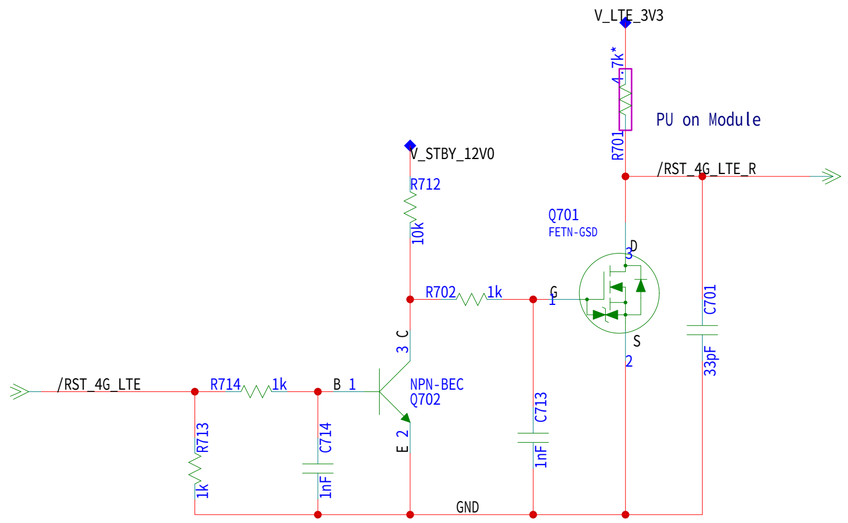
模块状态指示灯







RST



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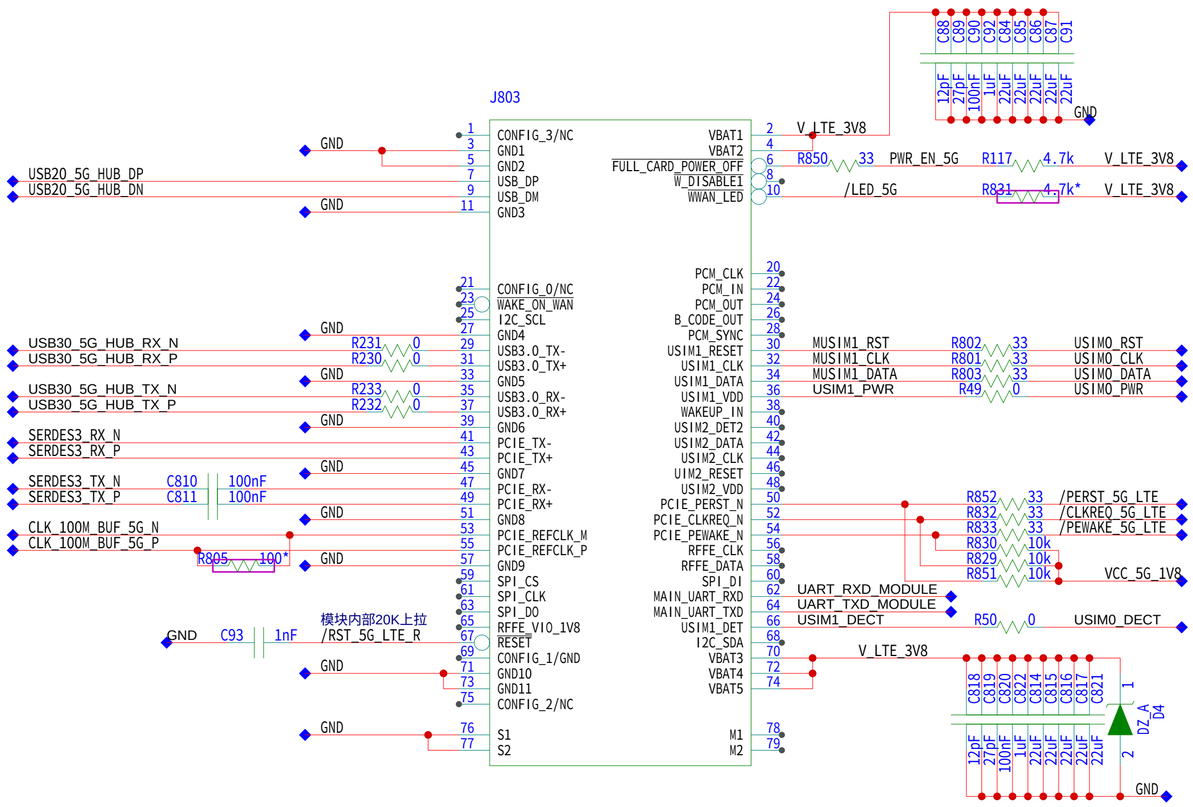
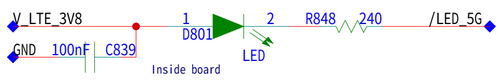
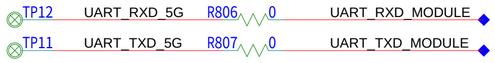
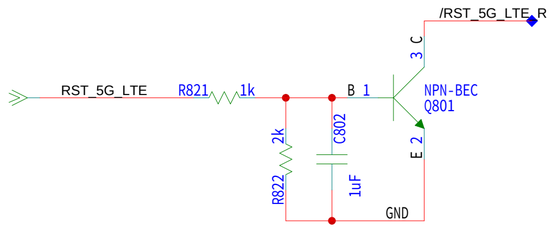
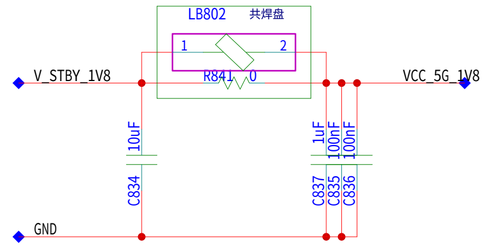
M.2-5G Module











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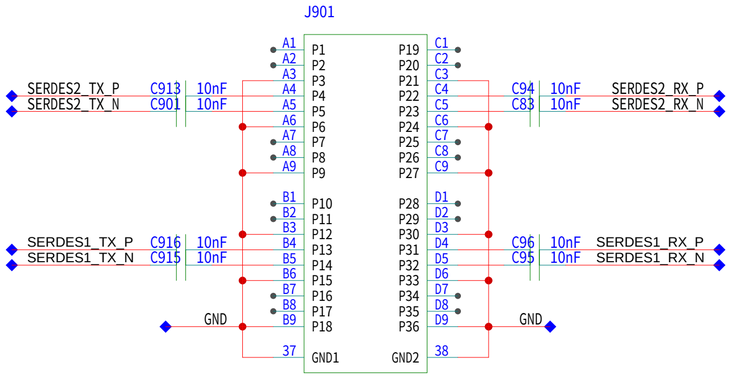
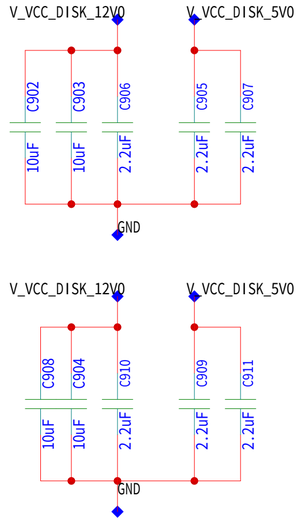
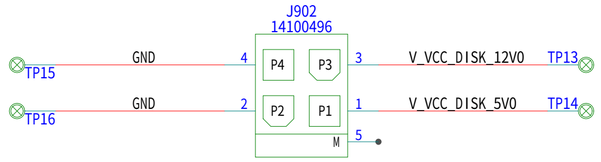
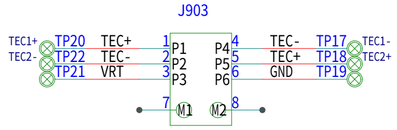


外接SATA硬盘



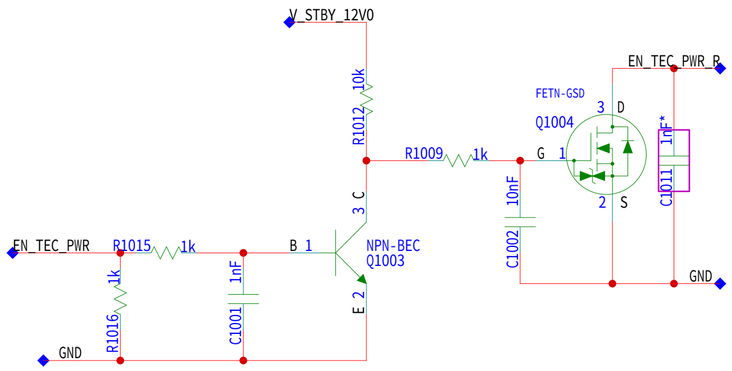
SATA硬盘供电

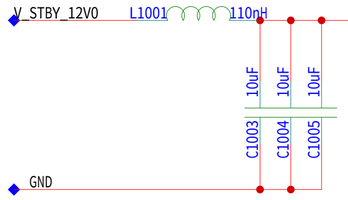


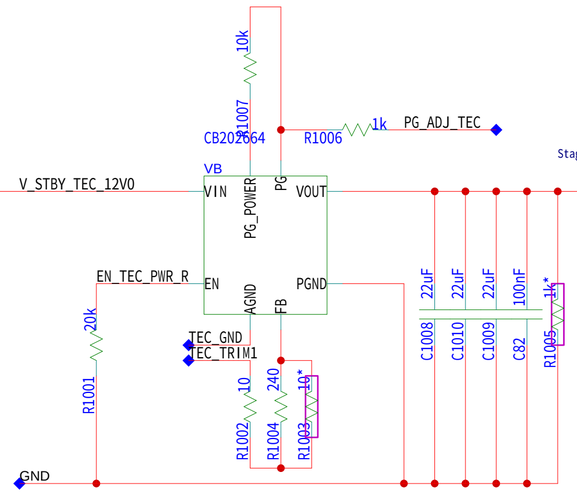


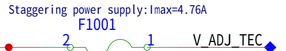
TEC为硬盘加热、降温模块

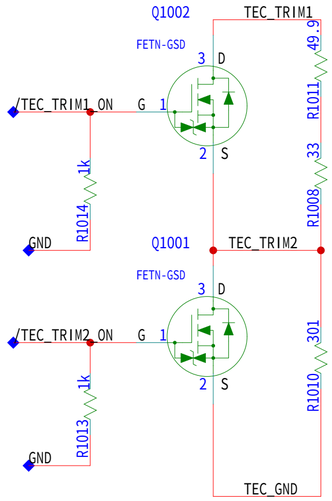
TEC_POWER





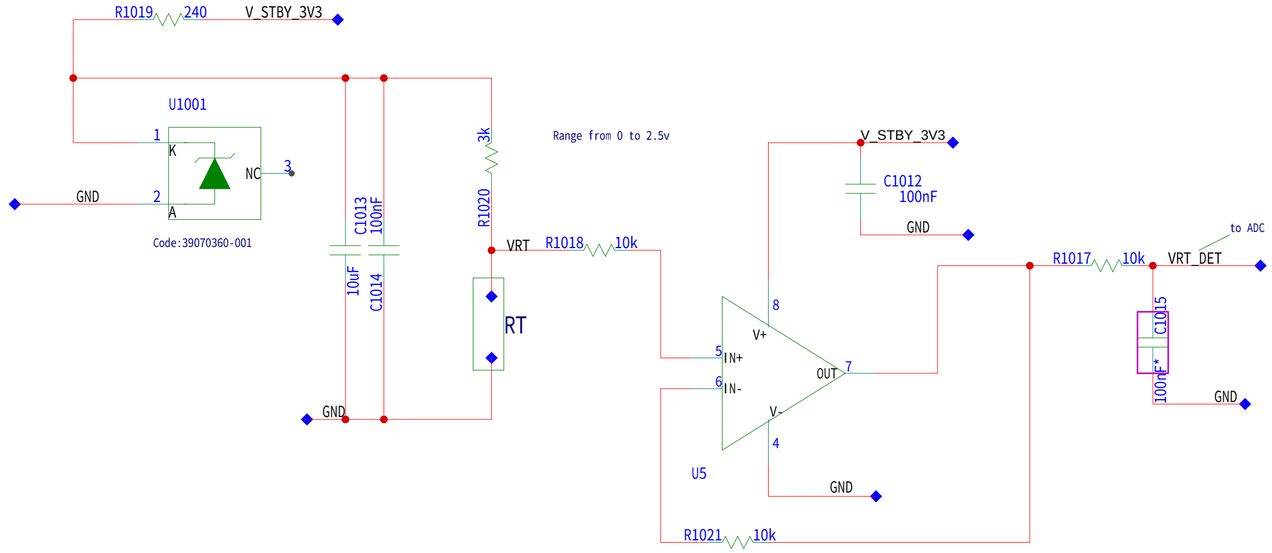


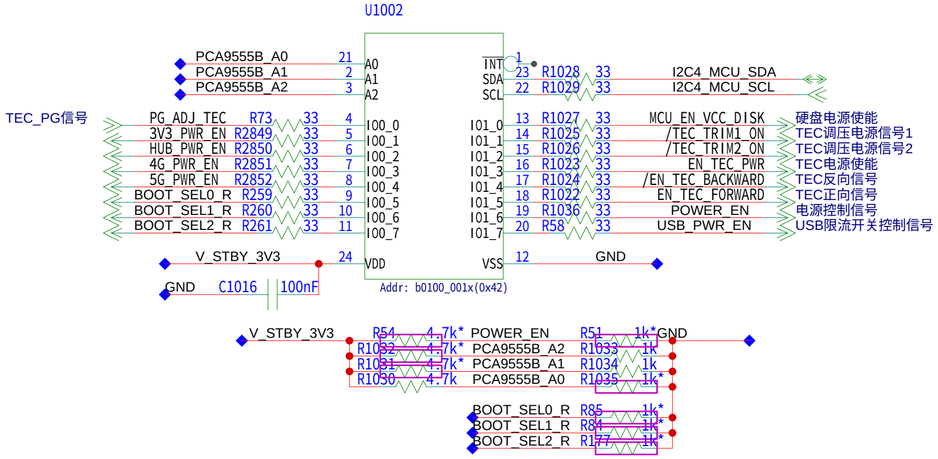




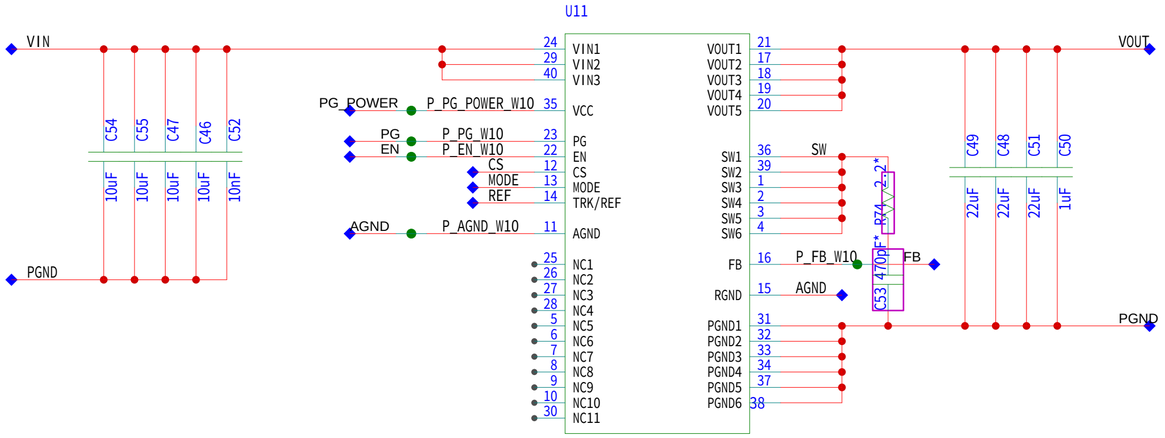
Vout = 0.6*(1+2/R)

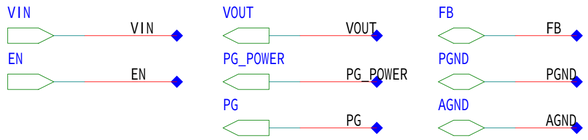
/TEC_TRIM1_ON	/TEC_TRIM2_ON	R	Vol
0	0	633.9 Ohm	2.49V
0	1	332.9 Ohm	4.20V
1	1	250 Ohm	5.4V





DC-DC CBB





NOTE:详细资料参考应用设计指导书

1、Vin：Cin最小值为20uF+10nF瓷片电容；

2、EN下拉电阻外置；在5V输出及以上场景时，CBB中EN下拉电阻R2001=17.4k（注：如要使用在5V输出以下场景，则需取R2001=20k）；该管脚不要外加电容

3、VCC:默认悬空，使用PG时必须上拉到该管脚（3V）

4、FB:输出调节，通过FB和RGND之间的电阻来调节输出电压，TRIM调节电阻R1和R2必须选择1%精度电阻。

5、PG:不使用PG时悬空，使用时上拉大于等于3K电阻至VCC（3V），且串联一个1K电阻至I/O口，不推荐外部电源（小于3.6V）上拉，外部上拉在EN使能前会有一个0.6V电平；

6、MODE:默认悬空，频率设定管脚

7、CS:默认悬空，OCP点设定管脚，过流点电阻Rcs（59K）已内置

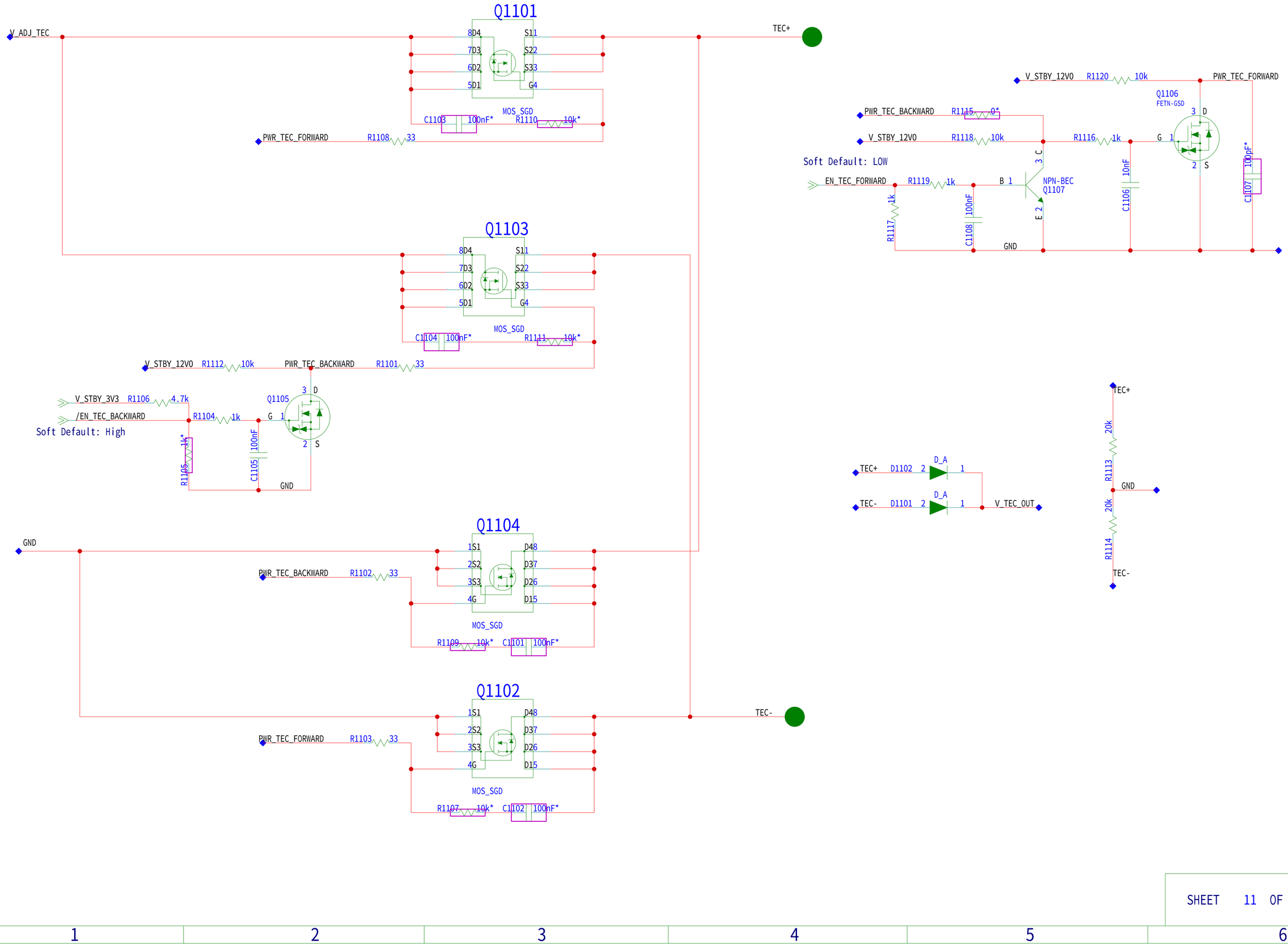
8、Vout：Cout最小值为44uF瓷片电容；

9、输出电压与输出电容配置见下表：输出电容选型，请与单板电源工程师讨论

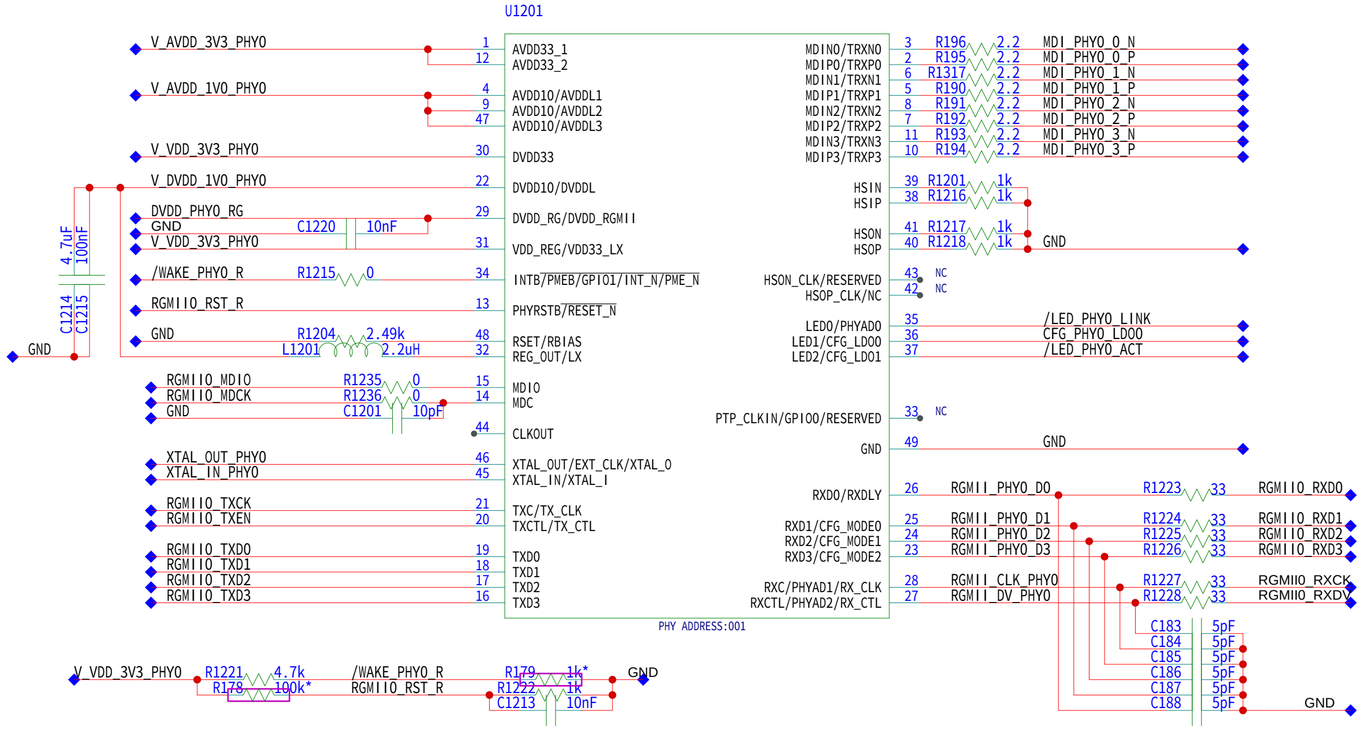
输出电压	0.7V	1.2V	1.8V	3.3V	5.4V
输出电源	9*22UF	7*22UF	5*22UF	4*22UF	3*22UF

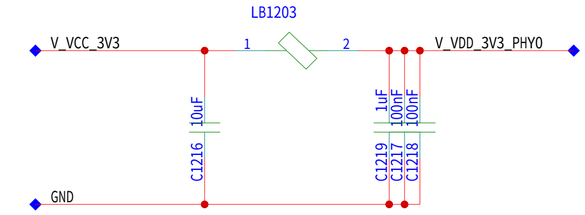
SHEET 1 OF 1

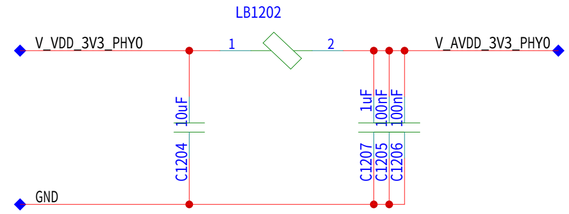
TEC_DRIVER（TEC为硬盘加热、降温模块）

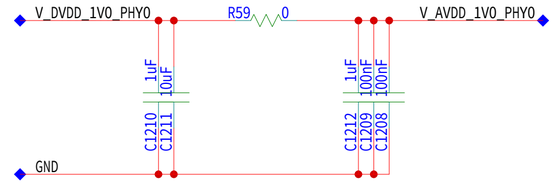


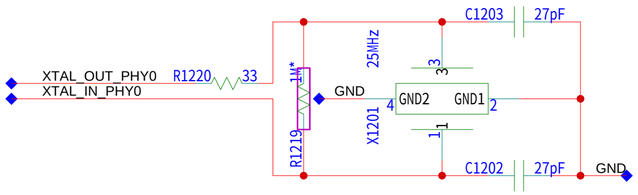
GE PHY











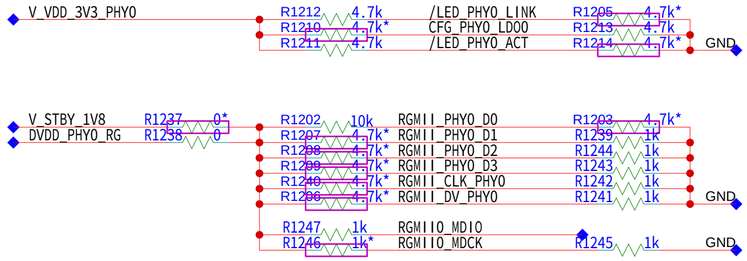
PIN	CFG		PIN	CFG
LED0	PHY_ADD0		RXD1	CFG_MODE0
RXC	PHY_ADD1		RXD2	CFG_MODE1
RXCTL	PHY_ADD2		RXD3	CFG_MODE2
RXD0	RXDLY			
LED1	CFG_LDO(0)			
LED2	CFG_LDO(1)			

10 CFG_LDO(1:0) LED2 LED1
STBY_12V0
01:2.5V
10:1.8V
11:1.5V

000 CFG_MODE[2:0] RXD3 RXD2 RXD1
000:UTP<-->RGMII
001:FIBER<-->RGMII
010:UTP/FIBER<-->RGMII
011:UTP<-->SGMII
100:SGMII(PHY)<-->RGMII(MAC)
101:SGMII(MAC)<-->RGMII(PHY)
110:UTP<-->FIBER(AUTO MODE)
111:UTP<-->FIBER(FORCE MODE)

011 PHY ADD[2:0] RXCTL RXC LED0

0* RXDLY RXD0
1: add 2ns dly to RXC for RXD 0：no delay



SHEET 12 OF 37

GE SWITCH

Boot Strap

DVDDIO
R1351 4.7k* POLED0
R1352 4.7k* POLED2
R1353 4.7k P1LED0
R1354 4.7k P1LED2
R1355 4.7k P2LED0
R1356 4.7k P2LED2
R1357 4.7k P3LED0
R1358 4.7k P3LED2
R1359 4.7k P4LED0
R1360 4.7k P4LED2
R1361 4.7k RTL8367_INT
R1370 4.7k
R1369 4.7k
R1368 4.7k*
R1367 4.7k*
R1371 4.7k*
R1366 4.7k*
R1365 4.7k*
R1363 4.7k*
R1364 4.7k*
R1362 4.7k*
R1372 1k*
GND

DVDDIO_1
R184 4.7k RGMII1_RXCK_R
R185 4.7k RGMII1_RXDV_R
R204 4.7k RGMII1_RXD0_R
R257 4.7k RGMII1_RXD1_R
R258 4.7k RGMII1_RXD2_R
R273 4.7k RGMII1_RXD3_R

POLED0/SMI_SEL
PULL UP:EEPROM SMI INTERFACE WHEN DIS_SPIS=1
**PULL DOWN:MII MANAGEMENT INTERFACE WHEN DIS_SPIS=1

POLED2/EN_PHY
**PULL UP:ENABLE EMBEDDED PHY
PULL DOWN:DISABLE EMBEDDED PHY

P1LED0/MIDO
PULL UP:MII PHY MANAGEMENT INTERFACE ID IS 29
**PULL DOWN:MII PHY MANAGEMENT INTERFACE ID IS 0

P1LED2/RESERVED
**MUST PULL HIGH OR KEEP FLOATING

P2LED0/DISAUTOLOAD
**PULL UP:DISABLE EEPROM AUTOLOAD
PULL DOWN:ENABLE EEPROM ANTULOAD

P2LED2/DIS_8051
**PULL UP:DISABLE 8051
PULL DOWN:ENABLE 8051

P3LED0/RESERVED
**MUST PULL LOW VIA 4.7K

P3LED2/EN_PWRLIGHT
**PULL UP:ENABLE POWER ON LIGHT
PULL DOWN:DISABLE POWER ON LIGHT

P4LED0/EEPROM_MOD
**PULL UP:24C32--24C256
PULL DOWN:24C02--24C16

P4LED2/DIS_SPI
**PULL UP:DISABLE SPI SLAVE
PULL DOWN:ENABLE SPI SLAVE

INTERRUPT
ACTIVE LOW BY PULL-UP TO DVDD VIA A 4.7K

LOOP DETECTION CONFIGURATION
**PULL UP:DISABLE LOOP DETECTION
PULL DOWN:ENABLE LOOP DETECTION

GND R1373 4.7k
RTL8367_INT
GND R1382 2.49k
/RTL8367_RST
GND R1374 4.7k
GND C1317 15pF RGMII1_TXCK
RGMII1_RXCK R1324 33 RGMII1_RXCK_R
GND C97 15pF
RGMII1_TXEN
RGMII1_RXDV R1323 33 RGMII1_RXDV_R
GND C189 5pF
RGMII1_TXD0
RGMII1_TXD1
RGMII1_TXD2
RGMII1_TXD3
RGMII1_RXD0 R1322 33 RGMII1_RXD0_R
GND C190 5pF
RGMII1_RXD1 R1321 33 RGMII1_RXD1_R
GND C191 5pF
RGMII1_RXD2 R1320 33 RGMII1_RXD2_R
GND C192 5pF
RGMII1_RXD3 R1318 33 RGMII1_RXD3_R
GND C193 5pF
GND R1375 4.7k
R1376 4.7k
R1377 4.7k
GND R1378 4.7k
R1379 4.7k
R1380 4.7k
R1381 4.7k

20 DIS_LPD/BUZZER
17 ATESTCK0
19 INTERRUPT
13 MDIREF
91 NRESET
15 RTT1
16 RTT2
56 E1_CRS/M1M_CRS
63 E1_DICLK/RG1_RXCLK/M1M_RXCLK
M1P_TXCLK
E1_GOCLK/RG1_TXCLK/M1M_TXCLK
M1P_RXCLK
E1_DIDV/RG1_RXCTL/M1M_RXDV
M1P_TXEN
E1_DOEN/RG1_TXCTL/M1M_TXEN
62 M1P_RXDV
64
61
65 E1_DIO/RG1_RXD0/M1M_RXD0
M1P_TXD0
66 E1_DI1/RG1_RXD1/M1M_RXD1
M1P_TXD1
67 E1_DI2/RG1_RXD2/M1M_RXD2
M1P_TXD2
68 E1_DI3/RG1_RXD3/M1M_RXD3
M1P_TXD3
60 E1_DO0/RG1_TXD0/M1M_TXD0
M1P_RXD0
59 E1_DO1/RG1_TXD1/M1M_TXD1
M1P_RXD1
58 E1_DO2/RG1_TXD2/M1M_TXD2
M1P_RXD2
57 E1_DO3/RG1_TXD3/M1M_TXD3
M1P_RXD3
47 E2_DICLK/RG2_RXCLK/M2M_RXCLK
M2P_TXCLK
46 E2_GOCLK/RG2_TXCLK/M2M_TXCLK
M2P_RXCLK
48 E2_DIDV/RG2_RXCTL/M2M_RXDV
M2P_TXEN
45 E2_DOEN/RG2_TXCTL/M2M_TXEN
M2P_RXDV
49 E2_DIO/RG2_RXD0/M2M_RXD0
M2P_TXD0
50 E2_DI1/RG2_RXD1/M2M_RXD1
M2P_TXD1
51 E2_DI2/RG2_RXD2/M2M_RXD2
M2P_TXD2
52 E2_DI3/RG2_RXD3/M2M_RXD3
M2P_TXD3
44 E2_DO0/RG2_TXD0/M2M_TXD0
M2P_RXD0
43 E2_DO1/RG2_TXD1/M2M_TXD1
M2P_RXD1
42 E2_DO2/RG2_TXD2/M2M_TXD2
M2P_RXD2
41 E2_DO3/RG2_TXD3/M2M_TXD3
M2P_RXD3

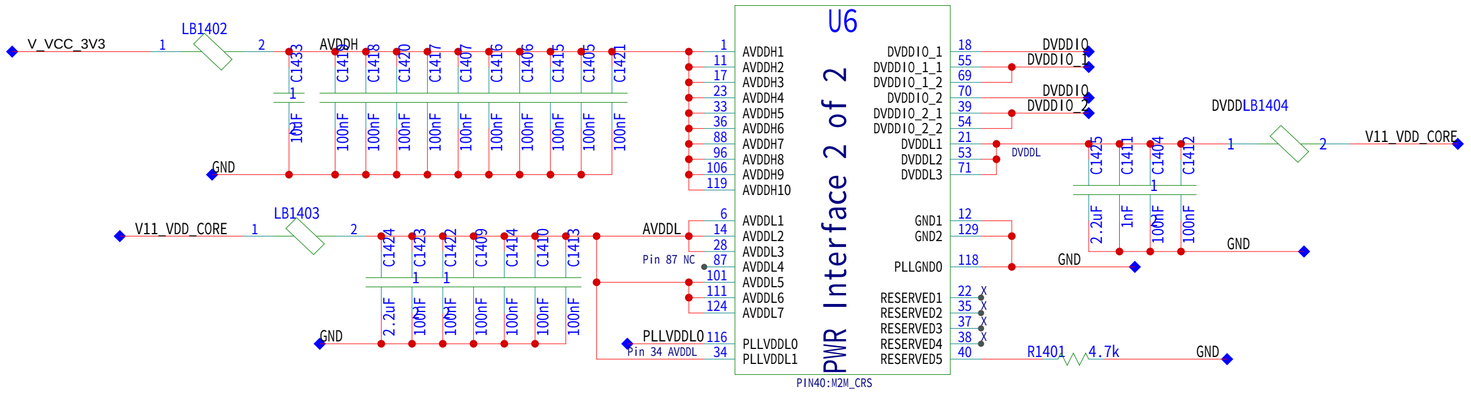
U6
MISC Interface 1 of 2

SPIS_CK/SCK/MMD_MDC 93 MDCK_V33
SPIS_CSI 92
SPIS_DI/SDA/MMD_MDIO 94 MDIO_V33
SPIS_DO 95
XTALI 90 8367_XTAL_IN
XTALO 89 8367_XTAL_OUT
C1318 27pF
C1319 27pF
X1301 25MHz
R1326 33
R1310 1M*
POLED0/LED_CK/SMI_SEL 86 POLED0
POLED1/LED_DA 85 X LED0
POLED2/EN_PHY 84 POLED2
POMDIAN 98 X 2
POMDIAP 97 X 1
POMDIBN 100 X 6
POMDIBP 99 X 3
POMDICN 103 X 5
POMDICP 102 X 4
POMDIDN 105 X 8
POMDIDP 104 X 7
P1LED0/RESERVED 82 P1LED0
P1LED1 83
P1LED2/RESERVED 81 P1LED2
P1MDIAN 108 CH1_TRXON_N R197 2.2 MDI_CH1_0_N C1316 3.9pF
P1MDIAP 107 CH1_TRXOP_PR1315 2.2 MDI_CH1_0_P C1310 3.9pF
P1MDIBN 110 CH1_TRX1N_NR1316 2.2 MDI_CH1_1_N C1311 3.9pF
P1MDIBP 109 CH1_TRX1P_PR1314 2.2 MDI_CH1_1_P C1312 3.9pF
P1MDICN 113 CH1_TRX2N_NR1313 2.2 MDI_CH1_2_N C1313 3.9pF
P1MDICP 112 CH1_TRX2P_PR1312 2.2 MDI_CH1_2_P C1314 3.9pF
P1MDIDN 115 CH1_TRX3N_NR1311 2.2 MDI_CH1_3_N C1315 3.9pF
P1MDIDP 114 CH1_TRX3P_PR1309 2.2 MDI_CH1_3_P C1309 3.9pF GND
P2LED0/DISAUTOLOAD 79 P2LED0
P2LED1 80
P2LED2/DIS_8051 78 P2LED2
P2MDIAN 121 CH2_TRXON_NR1308 2.2 MDI_CH2_0_N C1308 3.9pF
P2MDIAP 120 CH2_TRXOP_PR1307 2.2 MDI_CH2_0_P C1301 3.9pF
P2MDIBN 123 CH2_TRX1N_NR1306 2.2 MDI_CH2_1_N C1302 3.9pF
P2MDIBP 122 CH2_TRX1P_PR1305 2.2 MDI_CH2_1_P C1303 3.9pF
P2MDICN 126 CH2_TRX2N_NR1304 2.2 MDI_CH2_2_N C1304 3.9pF
P2MDICP 125 CH2_TRX2P_PR1303 2.2 MDI_CH2_2_P C1305 3.9pF
P2MDIDN 128 CH2_TRX3N_NR1302 2.2 MDI_CH2_3_N C1306 3.9pF
P2MDIDP 127 CH2_TRX3P_PR1301 2.2 MDI_CH2_3_P C1307 3.9pF GND
P3LED0/RESERVED 77 P3LED0
P3LED1 75
P3LED2/RESERVED 76 P3LED2
P3MDIAN 3 CH3_TRXONRN1335 2.2 MDI_CH3_0_N C1322 3.9pF
P3MDIAP 2 CH3_TRXOP_PR1336 2.2 MDI_CH3_0_P C1329 3.9pF
P3MDIBN 5 CH3_TRX1N_NR1337 2.2 MDI_CH3_1_N C1328 3.9pF
P3MDIBP 4 CH3_TRX1P_PR1338 2.2 MDI_CH3_1_P C1327 3.9pF
P3MDICN 8 CH3_TRX2N_NR1339 2.2 MDI_CH3_2_N C1326 3.9pF
P3MDICP 7 CH3_TRX2P_PR1340 2.2 MDI_CH3_2_P C1325 3.9pF
P3MDIDN 10 CH3_TRX3N_NR1341 2.2 MDI_CH3_3_N C1324 3.9pF
P3MDIDP 9 CH3_TRX3P_PR1342 2.2 MDI_CH3_3_P C1323 3.9pF GND
P4LED0/EEPROM_MOD 73 P4LED0
P4LED1 74
P4LED2/DIS_SPIS 72 P4LED2
P4MDIAN 25 CH4_TRXON_NR1343 2.2 MDI_CH4_0_N C1330 3.9pF
P4MDIAP 24 CH4_TRXOP_PR1344 2.2 MDI_CH4_0_P C1337 3.9pF
P4MDIBN 27 CH4_TRX1N_NR1345 2.2 MDI_CH4_1_N C1336 3.9pF
P4MDIBP 26 CH4_TRX1P_PR1346 2.2 MDI_CH4_1_P C1335 3.9pF
P4MDICN 30 CH4_TRX2N_NR1347 2.2 MDI_CH4_2_N C1334 3.9pF
P4MDICP 29 CH4_TRX2P_PR1348 2.2 MDI_CH4_2_P C1333 3.9pF
P4MDIDN 32 CH4_TRX3N_NR1349 2.2 MDI_CH4_3_N C1332 3.9pF
P4MDIDP 31 CH4_TRX3P_PR1350 2.2 MDI_CH4_3_P C1331 3.9pF GND

U1301
C1320 100nF GND
V_STBY_1V8
R1319 4.7k RGMII1_MDCK
R1325 4.7k RGMII1_MDIO
R1329 0
R1334 0
1 GND
2 VREF1
3 SCL1
4 SDA1
8 EN
7 VREF2
6 SCL2
5 SDA2
R1328 100k V_VCC_3V3
C1321 100nF GND
R1330 0 MDCK_V33
R1333 33 MDIO_V33
R1331 4.7k
R1332 4.7k
V_VCC_3V3

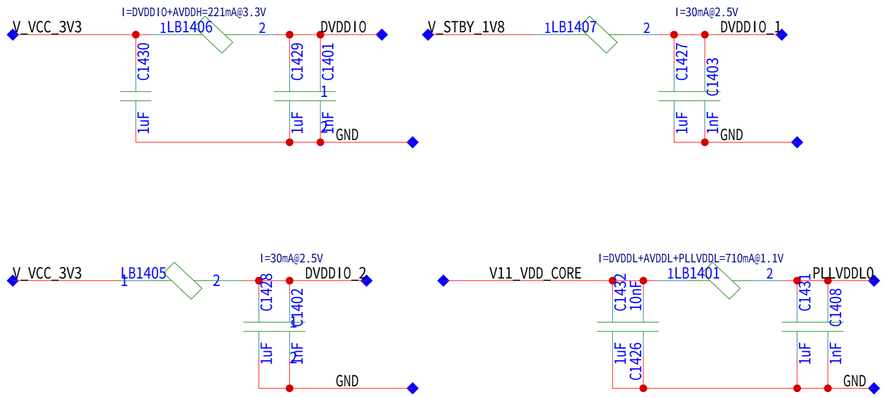
DVDDIO
R118 4.7k
/RTL8367_RST
tdelay=-RC*ln((E-V)/E)=9.3ms
C138 100nF
R121 1k*
GND

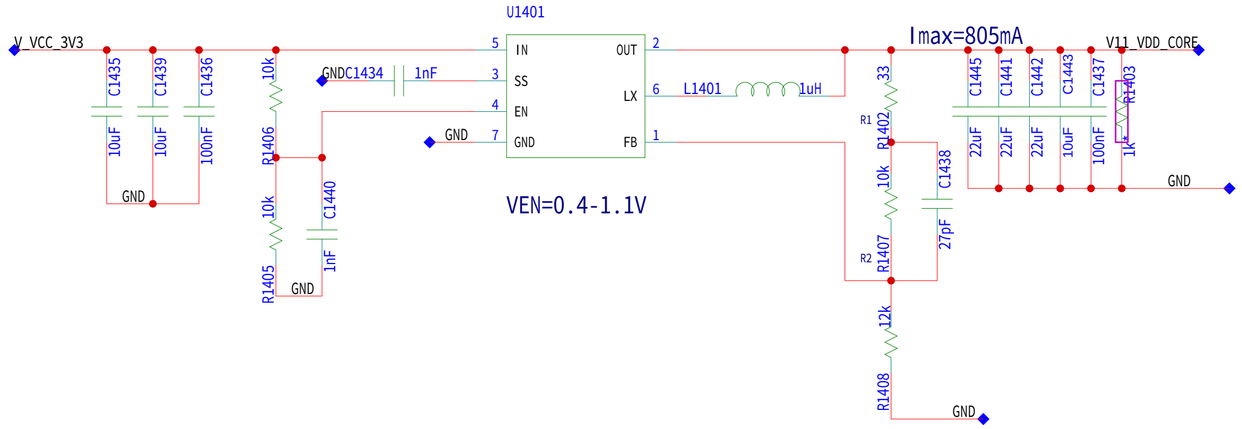
GE SWITCH PWR



DC/DC V33->V11_VDD_CORE

Vout=VREF*(1+R1/R2)=0.6*(1+10/12)=1.1V





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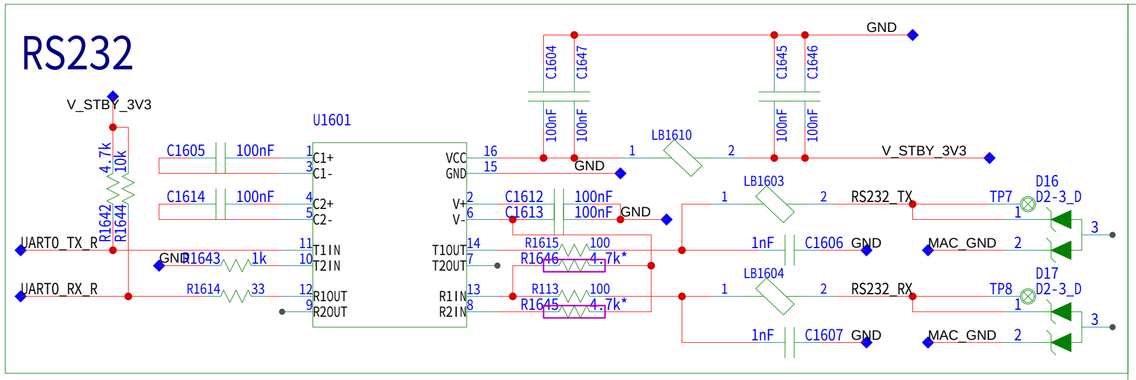
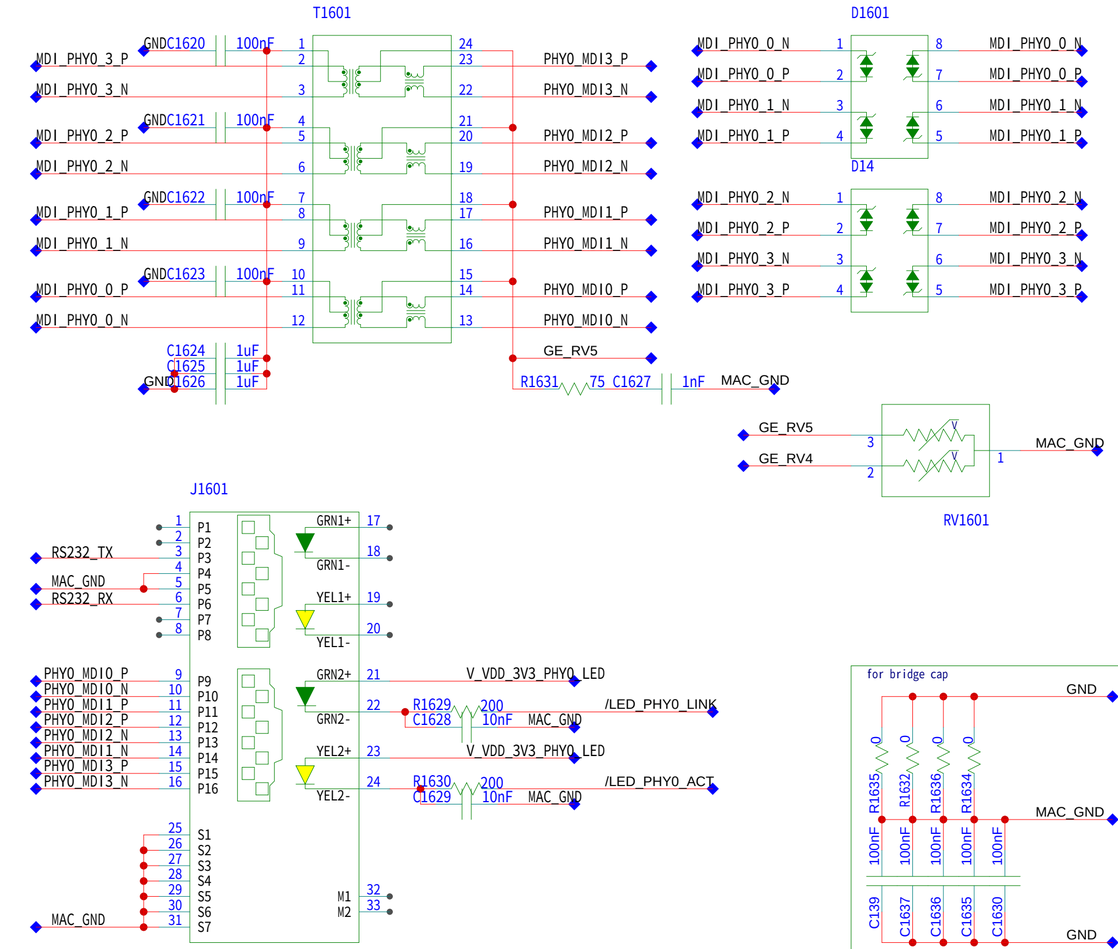
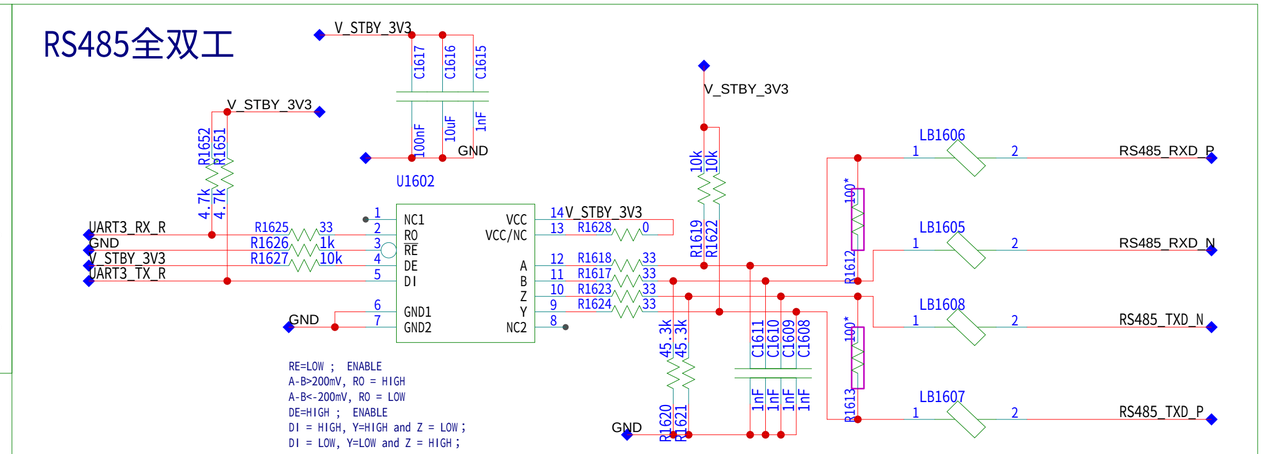
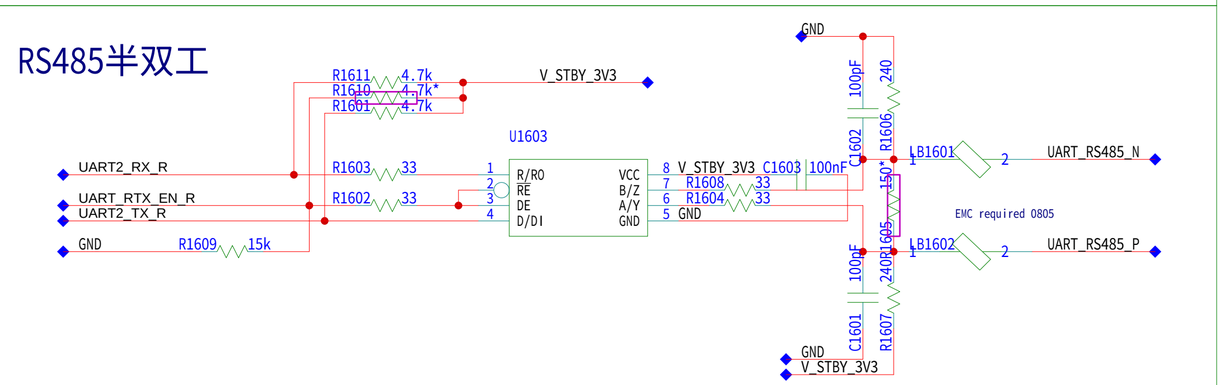
SHEET 15 OF 37

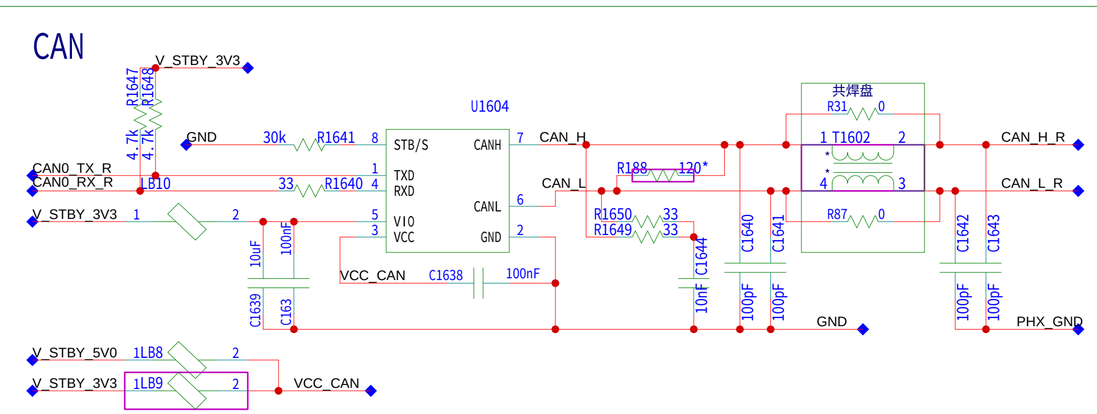

RS232
V_STBY_3V3
U1601
C1605 100nF
C1614 100nF
R1642 4.7k
R1644 10k
UART0_TX_R
UART0_RX_R
GND
R1643 1k
R1614 33
C1604 100nF
C1647 100nF
C1645 100nF
C1646 100nF
LB1610
LB1603
LB1604
C1612 100nF
C1613 100nF
R1615 100
R1646 4.7k*
R113 100
R1645 4.7k*
RS232_TX
RS232_RX
1nF C1606 GND
1nF C1607 GND
MAC_GND
TP7
TP8
D16 D2-3_D
D17 D2-3_D


T1601
D1601
D14
GNDC1620 100nF
GNDC1621 100nF
GNDC1622 100nF
GNDC1623 100nF
MDI_PHY0_3_P
MDI_PHY0_3_N
MDI_PHY0_2_P
MDI_PHY0_2_N
MDI_PHY0_1_P
MDI_PHY0_1_N
MDI_PHY0_0_P
MDI_PHY0_0_N
PHY0_MDI3_P
PHY0_MDI3_N
PHY0_MDI2_P
PHY0_MDI2_N
PHY0_MDI1_P
PHY0_MDI1_N
PHY0_MDI0_P
PHY0_MDI0_N
C1624 1uF
C1625 1uF
GND C1626 1uF
GE_RV5
R1631 75 C1627 1nF MAC_GND
GE_RV4
RV1601
J1601
RS232_TX
MAC_GND
RS232_RX
PHY0_MDI0_P
PHY0_MDI0_N
PHY0_MDI1_P
PHY0_MDI1_N
PHY0_MDI2_P
PHY0_MDI2_N
PHY0_MDI3_P
PHY0_MDI3_N
GRN1+
GRN1-
YEL1+
YEL1-
GRN2+
GRN2-
YEL2+
YEL2-
V_VDD_3V3_PHY0_LED
R1629 200
C1628 10nF MAC_GND
/LED_PHY0_LINK
R1630 200
C1629 10nF MAC_GND
/LED_PHY0_ACT

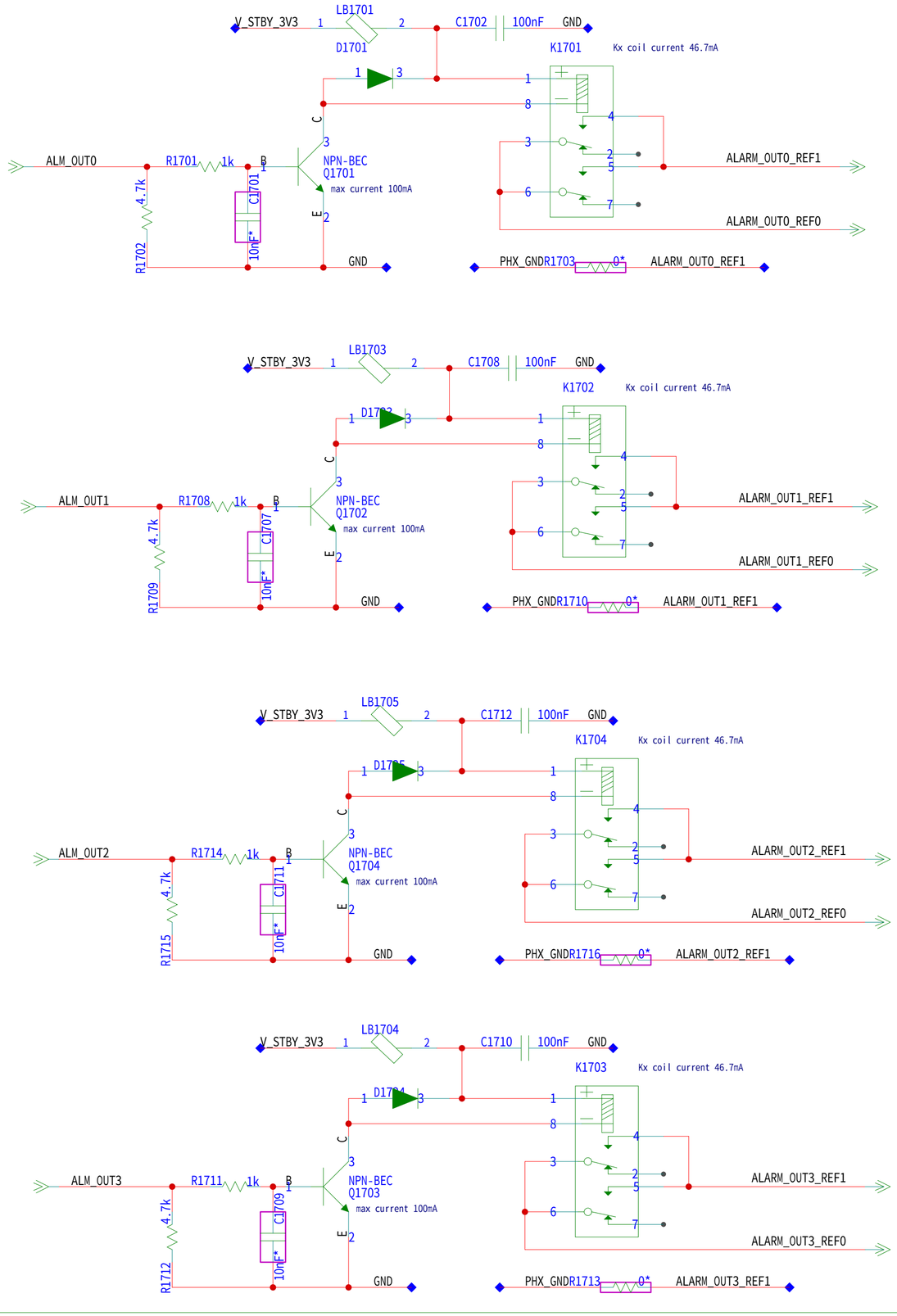
for bridge cap
R1635 0
R1632 0
R1636 0
R1634 0
100nF
C139
C1637
C1636
C1635
C1630
GND
MAC_GND
for bridge res
C1634
C1633
C1632
C1631
R1637 0
R1638 0
R1639 0
R1633 0
PHX_GND


RS485全双工
V_STBY_3V3
U1602
C1617
C1616
C1615
100nF
10uF
1nF
R1652 4.7k
R1651 4.7k
UART3_RX_R
UART3_TX_R
R1625 33
R1626 1k
R1627 10k
NC1
RO
RE
DE
DI
GND1
GND2
VCC
VCC/NC
A
B
Z
Y
NC2
R1628 0
R1618 33
R1617 33
R1623 33
R1624 33
R1619 10k
R1622 10k
45.3k
45.3k
R1620
R1621
C1611
C1610
C1609
C1608
1nF
R1612 100*
R1613 100*
LB1606
LB1605
LB1608
LB1607
RS485_RXD_P
RS485_RXD_N
RS485_TXD_N
RS485_TXD_P
RE=LOW ; ENABLE
A-B>200mV, RO = HIGH
A-B<-200mV, RO = LOW
DE=HIGH ; ENABLE
DI = HIGH, Y=HIGH and Z = LOW ;
DI = LOW, Y=LOW and Z = HIGH ;

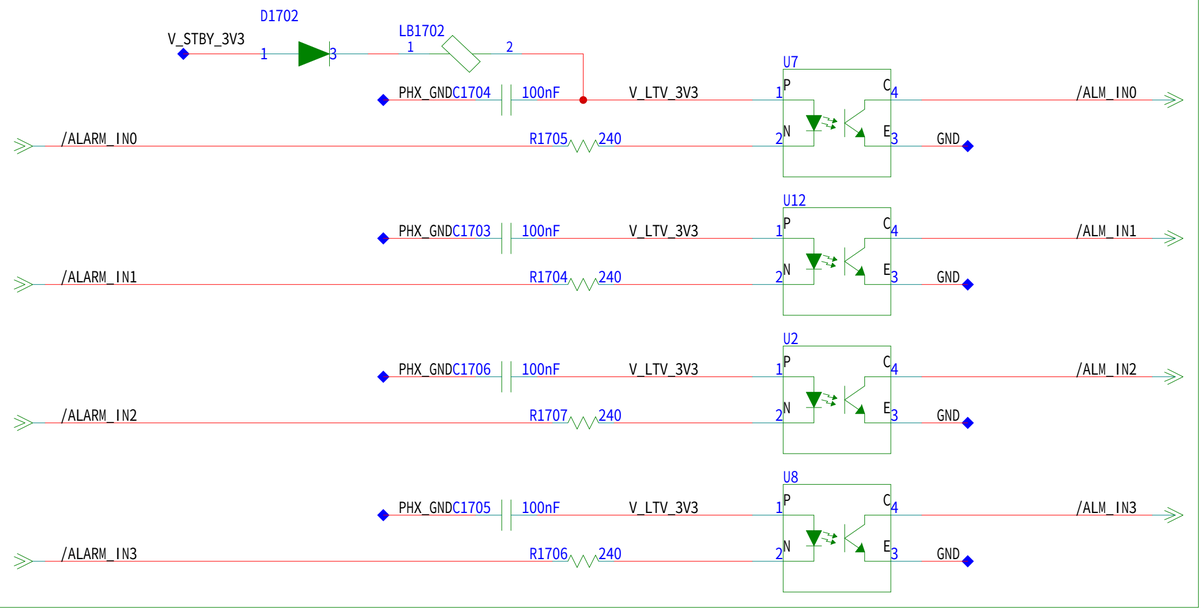

RS485半双工
R1611 4.7k
R1610 4.7k*
R1601 4.7k
V_STBY_3V3
U1603
UART2_RX_R
UART_RTX_EN_R
UART2_TX_R
GND
R1609 15k
R1603 33
R1602 33
R/RO
RE
DE
D/DI
VCC
B/Z
A/Y
GND
R1608 33
R1604 33
C1603 100nF
100pF
240
R1606
C1602
LB1601
LB1602
UART_RS485_N
UART_RS485_P
EMC required 0805
150*
R1605 240*
100nF
C1601
R1607

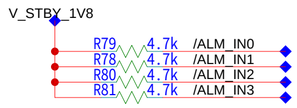

CAN
V_STBY_3V3
R1647 4.7k
R1648 4.7k
U1604
GND
30k R1641
CAN0_TX_R
CAN0_RX_R
LB10
33 R1640
V_STBY_3V3
10uF
100nF
C1639
C163
STB/S
TXD
RXD
VIO
VCC
CANH
CANL
GND
CAN_H
CAN_L
VCC_CAN
C1638 100nF
R188 120*
R1650 33
R1649 33
C1644 10nF
C1640
C1641
100pF
共焊盘
R31 0
T1602
R87 0
CAN_H_R
CAN_L_R
C1642
C1643
PHX_GND
V_STBY_5V0
1LB8
1LB9
VCC_CAN

ALARM 4 OUT

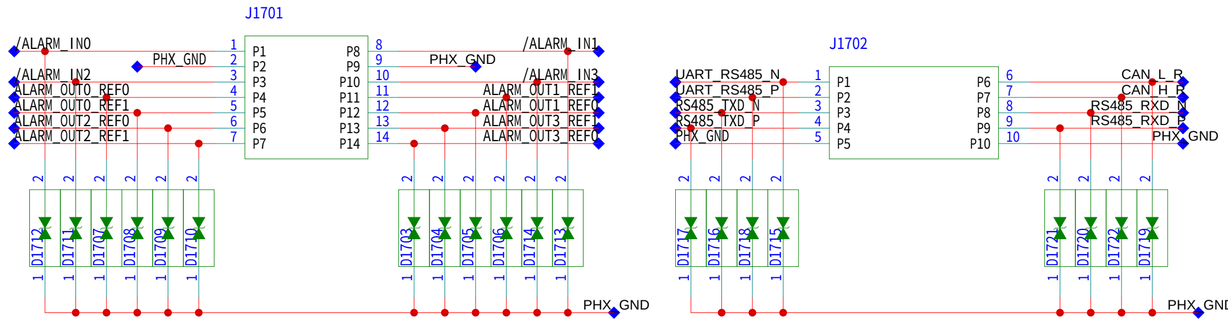


ALARM 4 IN



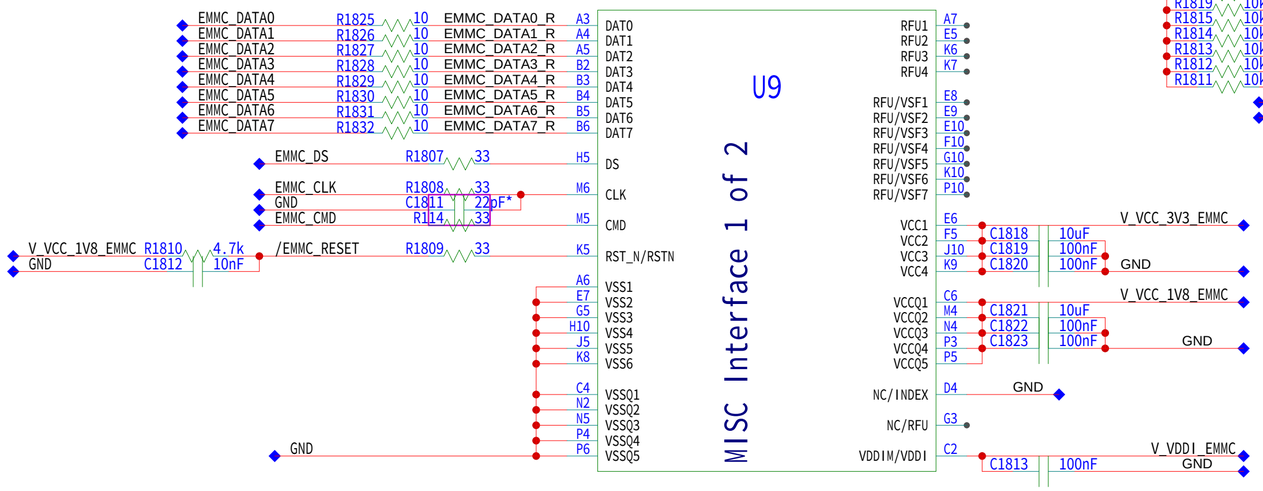


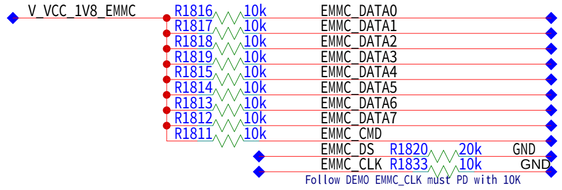
PHOENIX

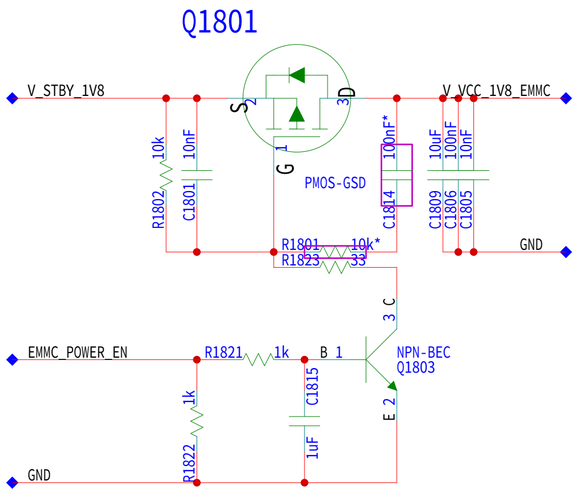


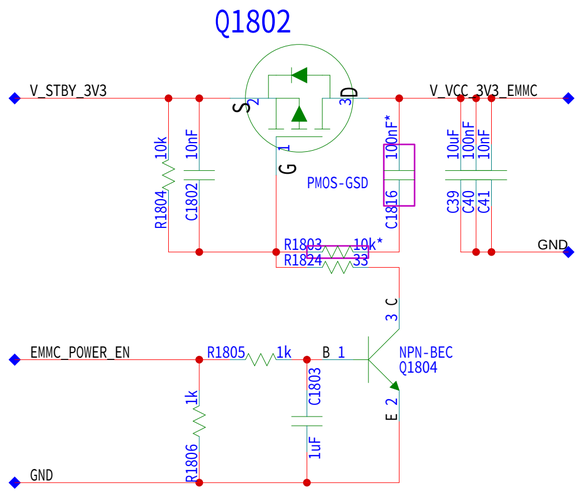
SHEET 17 OF 37

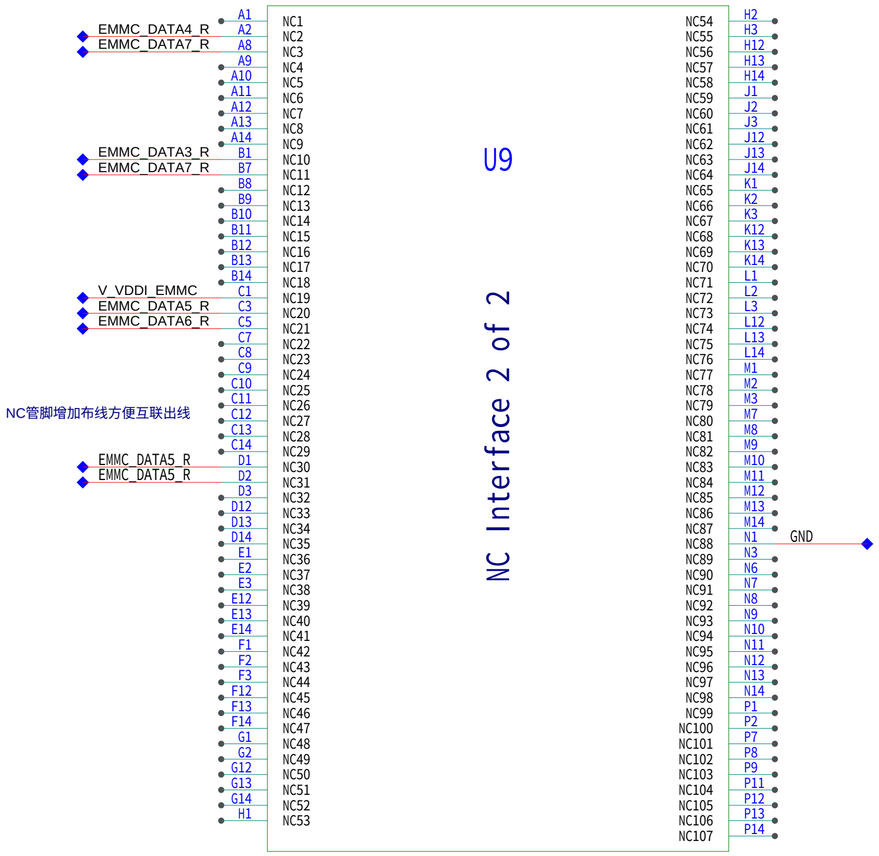
EMMC

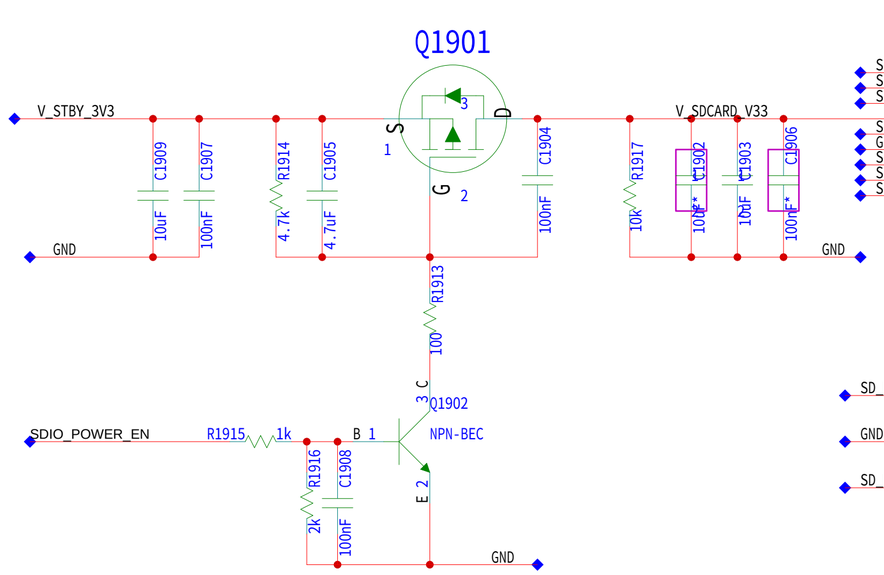

EMMC_DATA0
EMMC_DATA1
EMMC_DATA2
EMMC_DATA3
EMMC_DATA4
EMMC_DATA5
EMMC_DATA6
EMMC_DATA7
R1825 10 EMMC_DATA0_R
R1826 10 EMMC_DATA1_R
R1827 10 EMMC_DATA2_R
R1828 10 EMMC_DATA3_R
R1829 10 EMMC_DATA4_R
R1830 10 EMMC_DATA5_R
R1831 10 EMMC_DATA6_R
R1832 10 EMMC_DATA7_R
A3 A4 A5 B2 B3 B4 B5 B6
DAT0 DAT1 DAT2 DAT3 DAT4 DAT5 DAT6 DAT7
EMMC_DS R1807 33 H5
DS
EMMC_CLK R1808 33 M6
GND C1811 22pF*
CLK
EMMC_CMD R114 33 M5
CMD
V_VCC_1V8_EMMC R1810 4.7k
GND C1812 10nF
/EMMC_RESET R1809 33 K5
RST_N/RSTN
A6 E7 G5 H10 J5 K8
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6
C4 N2 N5 P4 P6
VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5
GND
U9
MISC Interface 1 of 2
RFU1 RFU2 RFU3 RFU4
A7 E5 K6 K7
RFU/VSF1 RFU/VSF2 RFU/VSF3 RFU/VSF4 RFU/VSF5 RFU/VSF6 RFU/VSF7
E8 E9 E10 F10 G10 K10 P10
VCC1 VCC2 VCC3 VCC4
E6 F5 J10 K9
C1818 10uF
C1819 100nF
C1820 100nF
V_VCC_3V3_EMMC
GND
VCCQ1 VCCQ2 VCCQ3 VCCQ4 VCCQ5
C6 M4 N4 P3 P5
C1821 10uF
C1822 100nF
C1823 100nF
V_VCC_1V8_EMMC
GND
NC/INDEX
D4
GND
NC/RFU
G3
VDDIM/VDDI
C2
C1813 100nF
V_VDDI_EMMC
GND

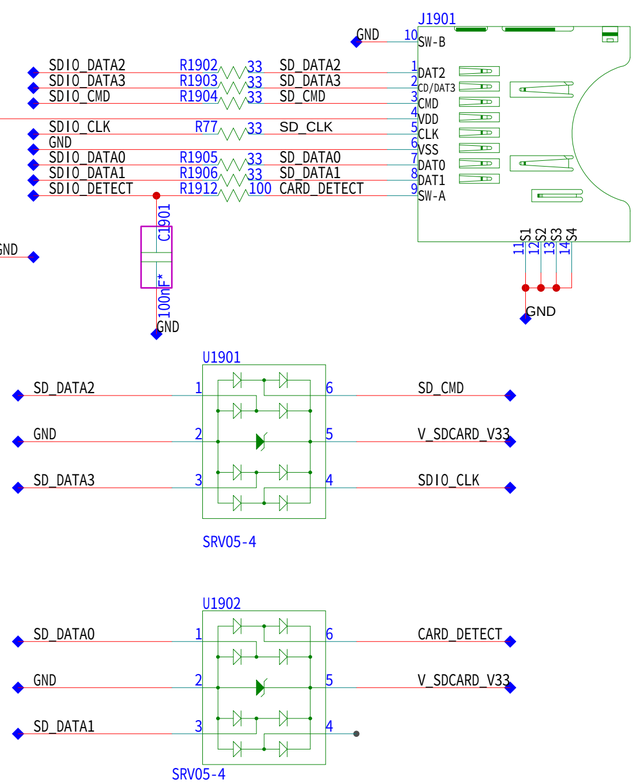

V_VCC_1V8_EMMC
R1816 10k EMMC_DATA0
R1817 10k EMMC_DATA1
R1818 10k EMMC_DATA2
R1819 10k EMMC_DATA3
R1815 10k EMMC_DATA4
R1814 10k EMMC_DATA5
R1813 10k EMMC_DATA6
R1812 10k EMMC_DATA7
R1811 10k EMMC_CMD
EMMC_DS R1820 20k GND
EMMC_CLK R1833 10k GND
Follow DEMO EMMC_CLK must PD with 10K

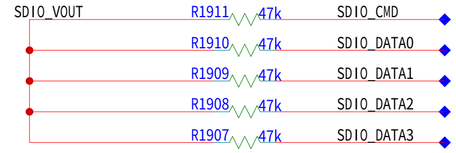

Q1801
V_STBY_1V8
R1802 10k
C1801 10nF
S 2
G 1
3 D
PMOS-GSD
C1814 100nF*
V_VCC_1V8_EMMC
C1809 10uF
C1806 100nF
C1805 10nF
GND
R1801 10k*
R1823 33
3 C
EMMC_POWER_EN
R1821 1k
B 1
NPN-BEC
Q1803
E 2
R1822 1k
C1815 1uF
GND

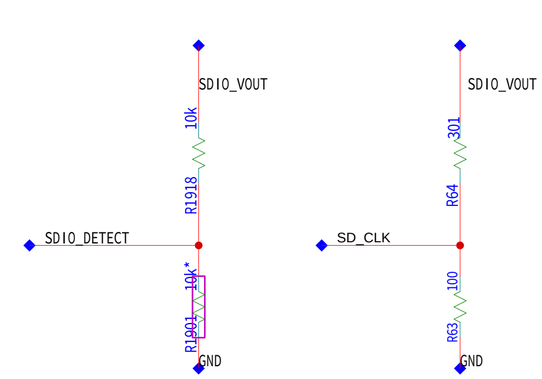

Q1802
V_STBY_3V3
R1804 10k
C1802 10nF
S 2
G 1
3 D
PMOS-GSD
C1816 100nF*
V_VCC_3V3_EMMC
C39 10uF
C40 100nF
C41 10nF
GND
R1803 10k*
R1824 33
3 C
EMMC_POWER_EN
R1805 1k
B 1
NPN-BEC
Q1804
E 2
R1806 1k
C1803 1uF
GND


EMMC_DATA4_R
EMMC_DATA7_R
EMMC_DATA3_R
EMMC_DATA7_R
V_VDDI_EMMC
EMMC_DATA5_R
EMMC_DATA6_R
NC管脚增加布线方便互联出线
EMMC_DATA5_R
EMMC_DATA5_R
A1 A2 A8 A9 A10 A11 A12 A13 A14
B1 B7 B8 B9 B10 B11 B12 B13 B14
C1 C3 C5 C7 C8 C9 C10 C11 C12 C13 C14
D1 D2 D3 D12 D13 D14 E1 E2 E3 E12 E13 E14 F1 F2 F3 F12 F13 F14 G1 G2 G12 G13 G14 H1
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16 NC17 NC18 NC19 NC20 NC21 NC22 NC23 NC24 NC25 NC26 NC27 NC28 NC29 NC30 NC31 NC32 NC33 NC34 NC35 NC36 NC37 NC38 NC39 NC40 NC41 NC42 NC43 NC44 NC45 NC46 NC47 NC48 NC49 NC50 NC51 NC52 NC53
U9
NC Interface 2 of 2
NC
NC54 NC55 NC56 NC57 NC58 NC59 NC60 NC61 NC62 NC63 NC64 NC65 NC66 NC67 NC68 NC69 NC70 NC71 NC72 NC73 NC74 NC75 NC76 NC77 NC78 NC79 NC80 NC81 NC82 NC83 NC84 NC85 NC86 NC87 NC88 NC89 NC90 NC91 NC92 NC93 NC94 NC95 NC96 NC97 NC98 NC99 NC100 NC101 NC102 NC103 NC104 NC105 NC106 NC107
H2 H3 H12 H13 H14 J1 J2 J3 J12 J13 J14 K1 K2 K3 K12 K13 K14 L1 L2 L3 L12 L13 L14 M1 M2 M3 M7 M8 M9 M10 M11 M12 M13 M14 N1 N3 N6 N7 N8 N9 N10 N11 N12 N13 N14 P1 P2 P7 P8 P9 P11 P12 P13 P14
GND



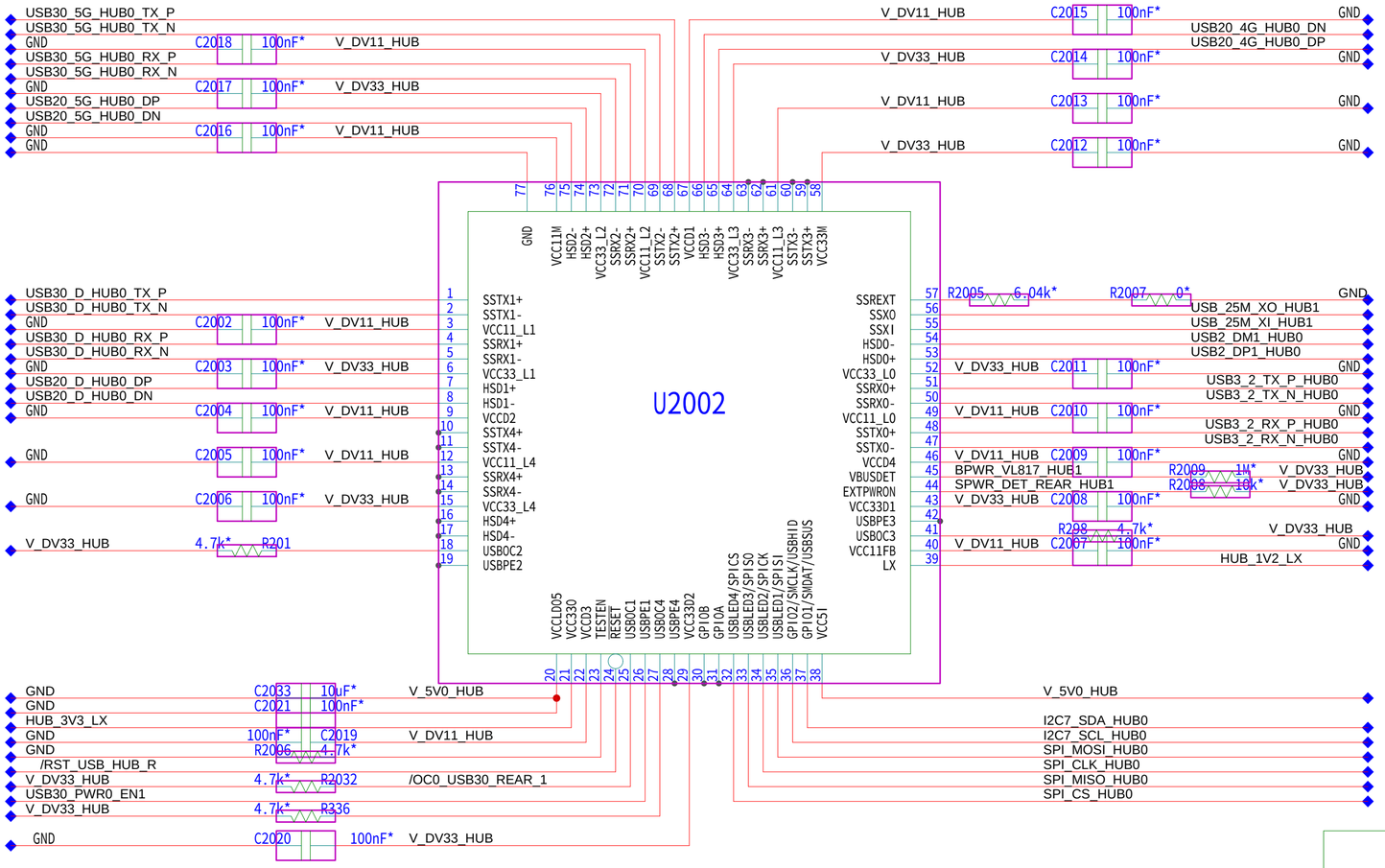


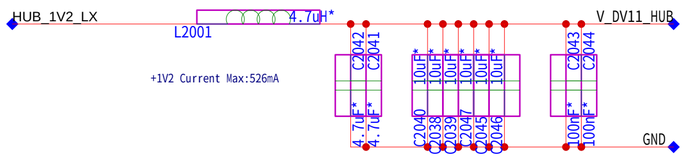


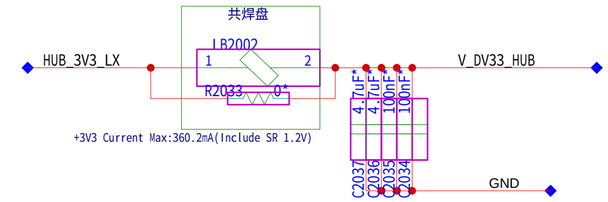


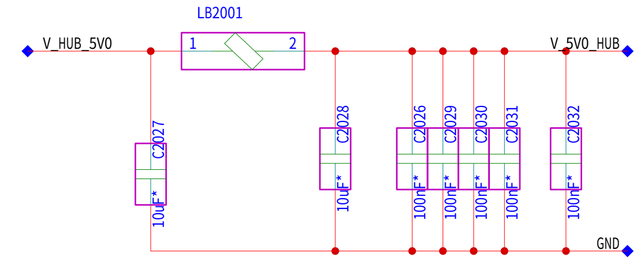
SDIO_DETECT和SD_CLK一定要按这个方案设计

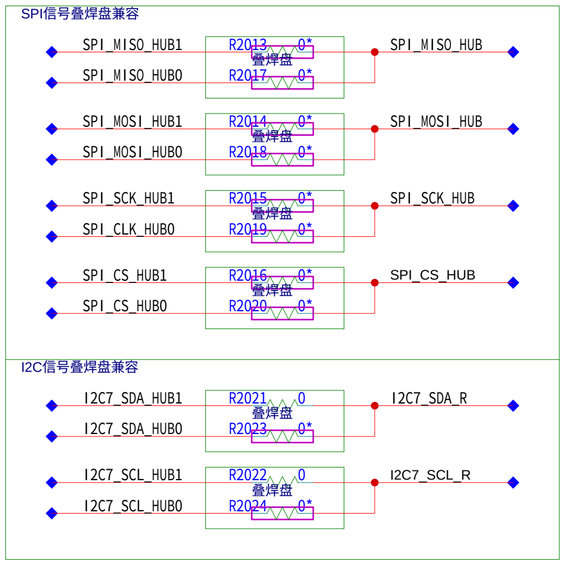
USB3.0 & USB2.0 HUB（兼容设计，此方案不上件）

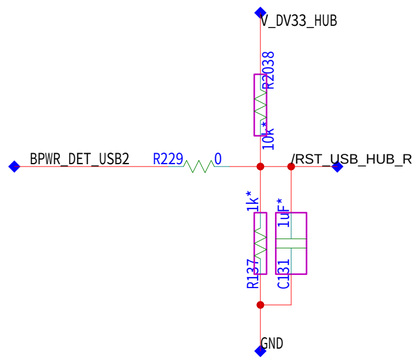


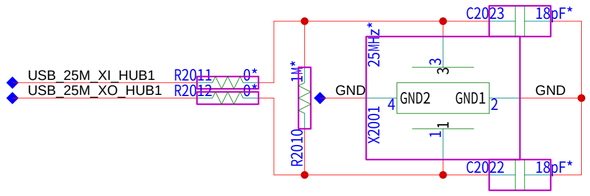


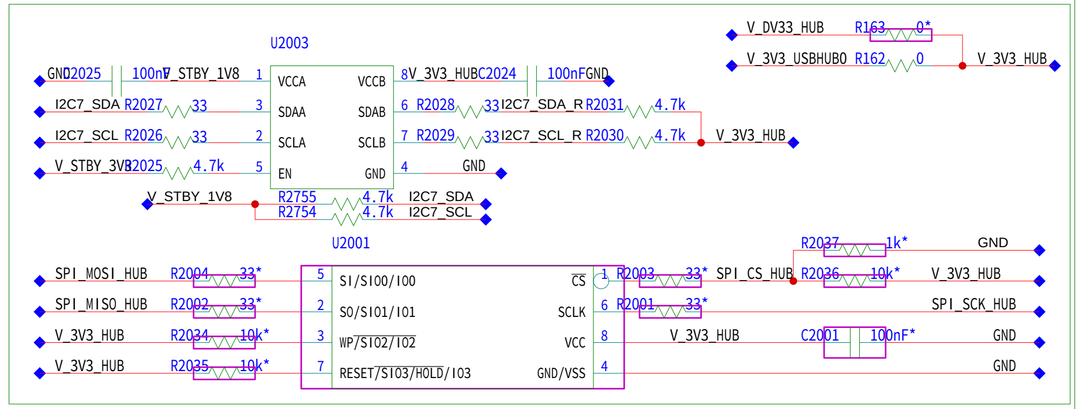




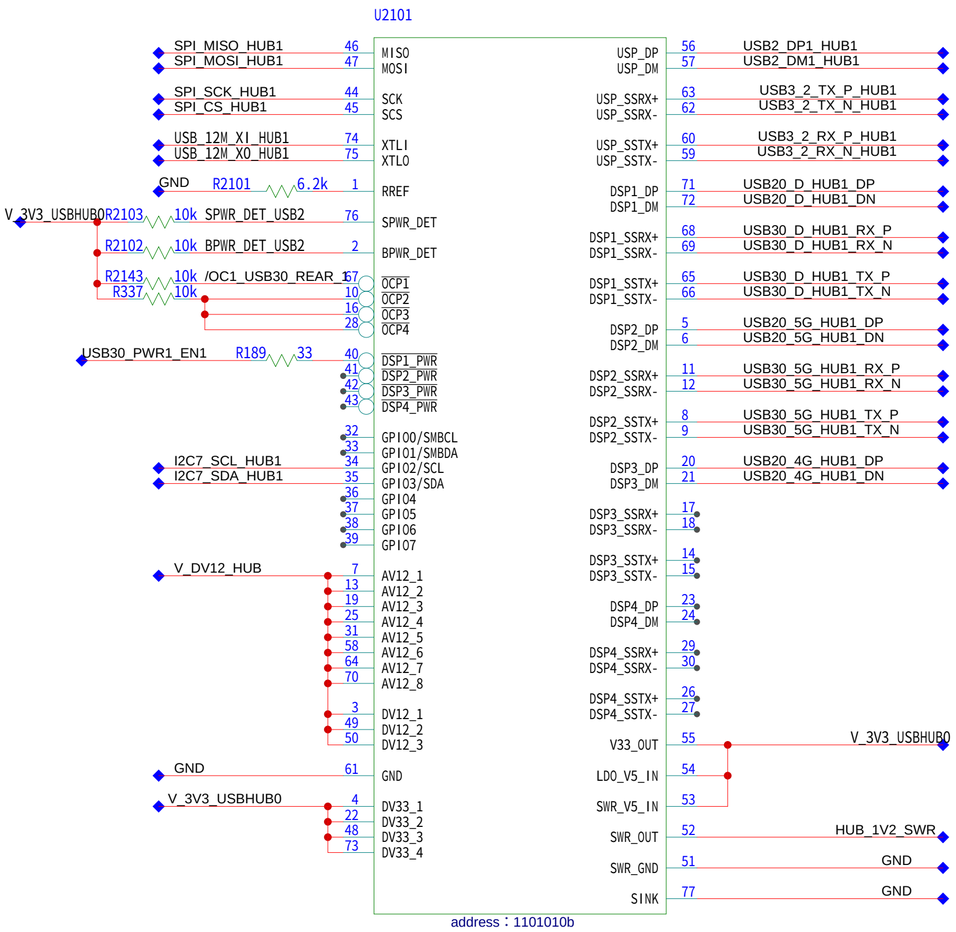




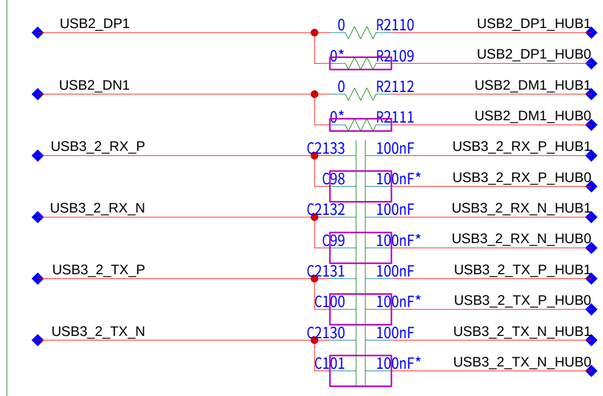


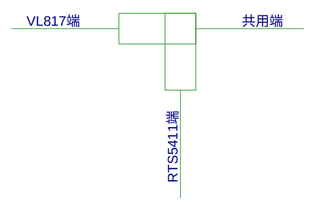


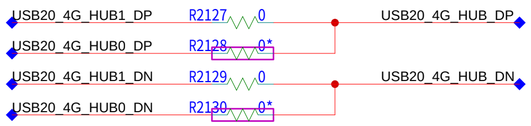
USB3.0 & USB2.0 HUB CHOSE

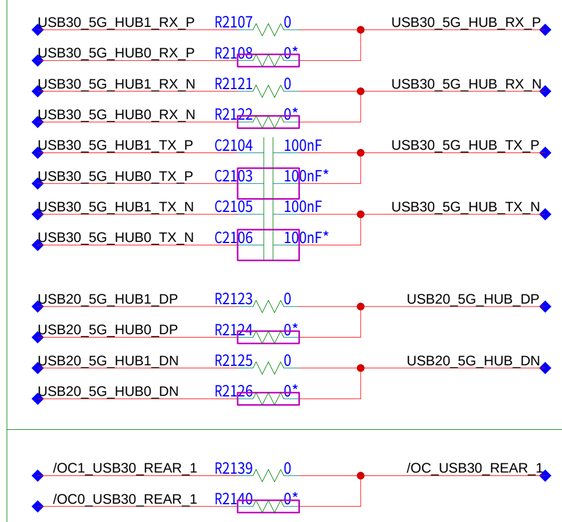


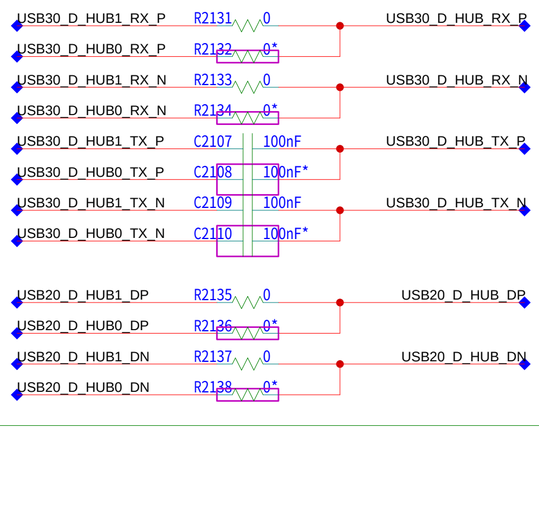
USB HUB方案兼容，做分叉叠焊盘设计

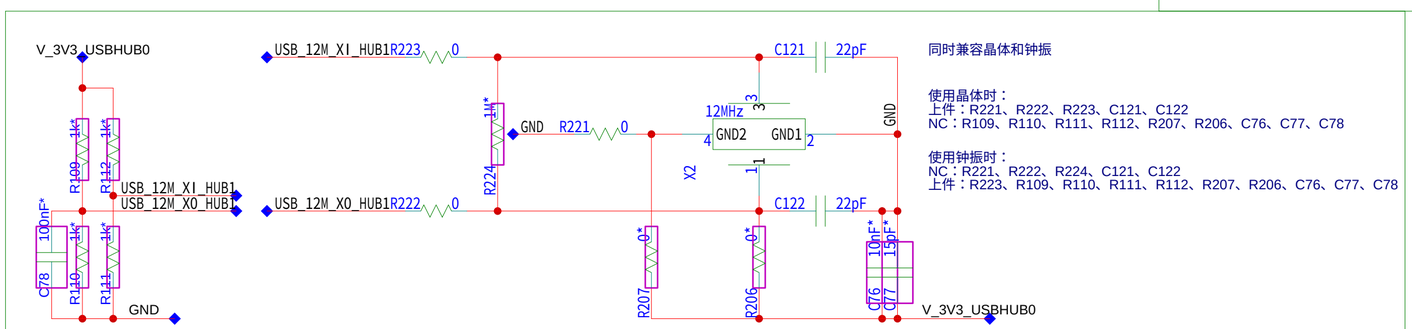


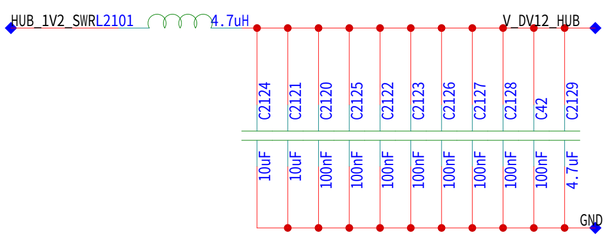


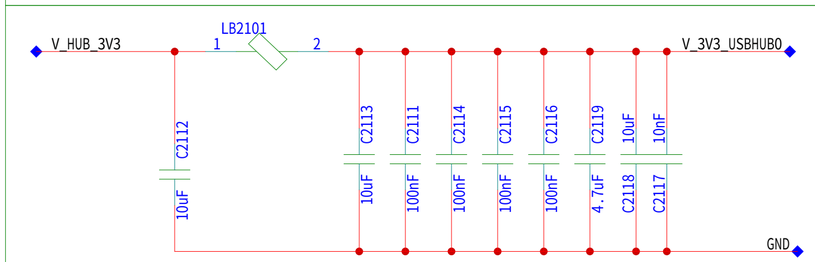


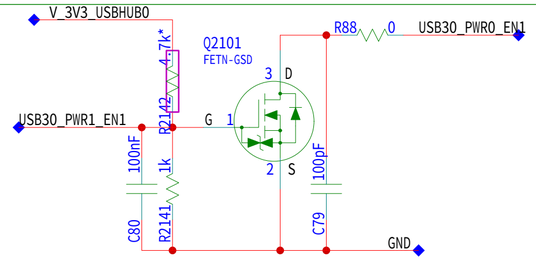












两种HUB的PWR控制逻辑相反，需要兼容两种高低电平逻辑进行设计；

SHEET 21 OF 37

USB3.0 + USB2.0 Connector + Dongle(Type-A)

共焊盘

R2212 0
R2211 0
T2202
USB30_D_HUB_TX_N → USB30_D_HUB_CONN_TX_N
USB30_D_HUB_TX_P → USB30_D_HUB_CONN_TX_P

R2209 0
R2210 0
T2201
USB30_D_HUB_RX_N → USB30_D_HUB_CONN_RX_N
USB30_D_HUB_RX_P → USB30_D_HUB_CONN_RX_P

R2218 0
R2219 0
T2203
USB20_D_HUB_DN → USB20_D_HUB_CONN_DN
USB20_D_HUB_DP → USB20_D_HUB_CONN_DP

R2220 0
R2221 0
T2204
USB2_DN2 → USB2_CONN_DN2
USB2_DP2 → USB2_CONN_DP2

R2230 0
R2231 0
T2209
USB2_DN3 → USB2_CONN_DN3
USB2_DP3 → USB2_CONN_DP3

共焊盘

R2225 0
R2224 0
T2206
USB3_1_RX_N → USB3_1_CONN_RX_N
USB3_1_RX_P → USB3_1_CONN_RX_P

R2222 0
R2223 0
T2205
USB3_1_TX_N C127 100nF → USB3_1_CONN_TX_N
USB3_1_TX_P C128 100nF → USB3_1_CONN_TX_P

R2226 0
R2227 0
T2207
USB3_0_RX_N → USB3_0_CONN_RX_N
USB3_0_RX_P → USB3_0_CONN_RX_P

R2228 0
R2229 0
T2208
USB3_0_TX_N C123 100nF → USB3_0_CONN_TX_N
USB3_0_TX_P C124 100nF → USB3_0_CONN_TX_P

D2203
USB3_1_CONN_RX_N
USB3_1_CONN_RX_P
GND
USB3_1_CONN_TX_N
USB3_1_CONN_TX_P
I/O_1 I/O_2 I/O_3 I/O_4 VSS1 VSS2 NC1 NC2 NC3 NC4

U2205
USB2_CONN_DN3 → USB2_CONN_DN2
GND
USB2_CONN_DP3 → USB2_CONN_DP2
SRV05-4

D2202
USB3_0_CONN_RX_N
USB3_0_CONN_RX_P
GND
USB3_0_CONN_TX_N
USB3_0_CONN_TX_P
I/O_1 I/O_2 I/O_3 I/O_4 VSS1 VSS2 NC1 NC2 NC3 NC4

U2206
USB20_D_HUB_CONN_DN
GND
USB20_D_HUB_CONN_DP
USB3_5V0
SRV05-4

D2201
USB30_D_HUB_CONN_TX_P
USB30_D_HUB_CONN_TX_N
GND
USB30_D_HUB_CONN_RX_P
USB30_D_HUB_CONN_RX_N
I/O_1 I/O_2 I/O_3 I/O_4 VSS1 VSS2 NC1 NC2 NC3 NC4

对外USB3.0接口

J2201
USB1_5V0 → VBUS
USB2_CONN_DN2 R251 0 → D-
USB2_CONN_DP2 R252 0 → D+
GND → PGND
USB3_1_CONN_RX_N → SSRX-
USB3_1_CONN_RX_P → SSRX+
GND
USB3_1_CONN_TX_N → SSTX-
USB3_1_CONN_TX_P → SSTX+
GND → S1, S2

J2202
USB2_5V0 → VBUS
USB2_CONN_DN3 R253 0 → D-
USB2_CONN_DP3 R254 0 → D+
GND → PGND
USB3_0_CONN_RX_N → SSRX-
USB3_0_CONN_RX_P → SSRX+
GND
USB3_0_CONN_TX_N → SSTX-
USB3_0_CONN_TX_P → SSTX+
GND → S1, S2

内部加密狗接口

J2203
USB3_5V0 → VBUS
USB20_D_HUB_CONN_DN → D-
USB20_D_HUB_CONN_DP → D+
GND → PGND
USB30_D_HUB_CONN_RX_N → SSRX-
USB30_D_HUB_CONN_RX_P → SSRX+
GND
USB30_D_HUB_CONN_TX_N → SSTX-
USB30_D_HUB_CONN_TX_P → SSTX+
GND → S1, S2

U2201
V_STBY_5V0
R2203 10k*
USB_PWR_EN
C161 10uF
GND
VIN VOUT GND ILIM EN FLG/FAULT SINK
1LB2201
R2202 11.3K
R2201 5.6k
C56 C57 C58 C59 C60 22uF
C73 100nF
C2202 10uF
R2204 10k
D9
USB1_5V0
I limit=1.5A(16.9K)

U2202
V_STBY_5V0
R2207 10k
USB_PWR_EN
C160 10uF
GND
VIN VOUT GND ILIM EN FLG/FAULT SINK
1LB2202
R2206 11.3K
R2205 5.6k
C61 C62 C63 C64 C65 22uF
C71 100nF
C2206 10uF
R2208 10k
D7
USB2_5V0
I limit=1.5A(16.9K)

U2203
V_STBY_5V0
R238 10k
USB30_PWR0_EN1
R2217 10k*
C159 10uF
GND
VIN VOUT GND ILIM EN FLG/FAULT SINK
1LB2203
R2214 11.3K
R2213 5.6k
R2215 10k
V_STBY_3V3
/OC_USB30_REAR_1
C66 C67 C68 C69 C70 22uF
C72 100nF
C2210 10uF
R2216 10k
D8
USB3_5V0
I limit=1.5A(16.9K)

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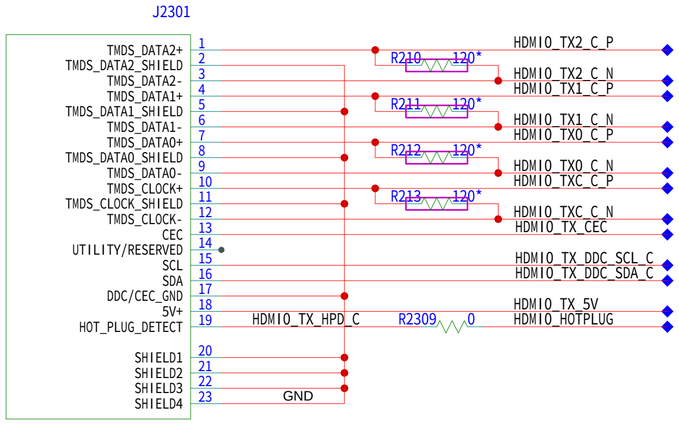
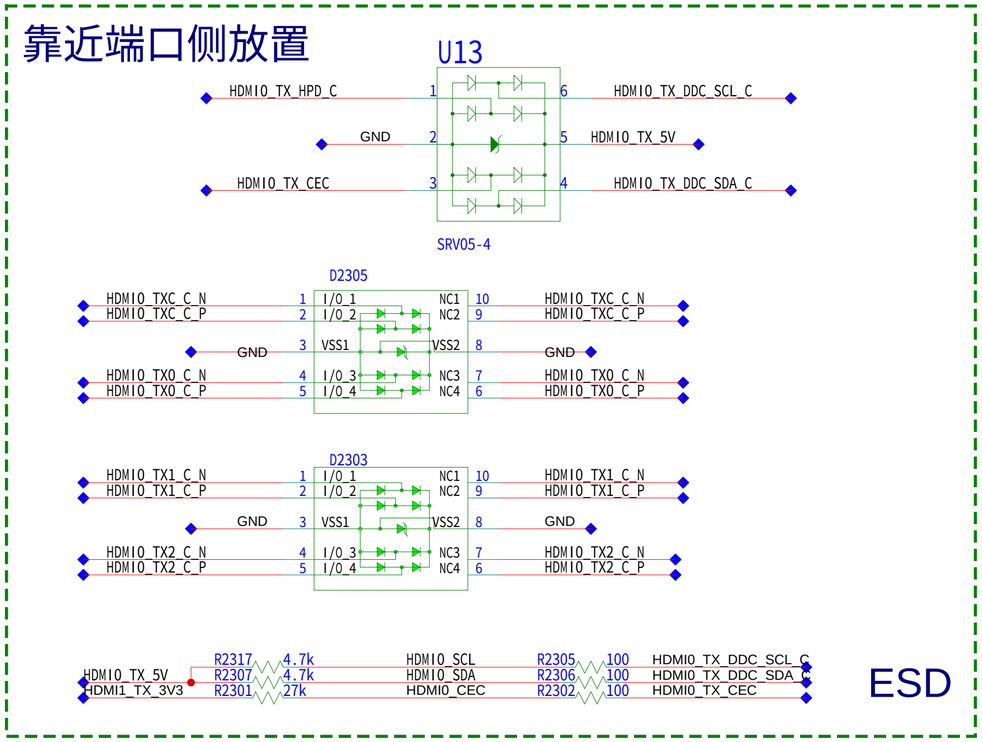
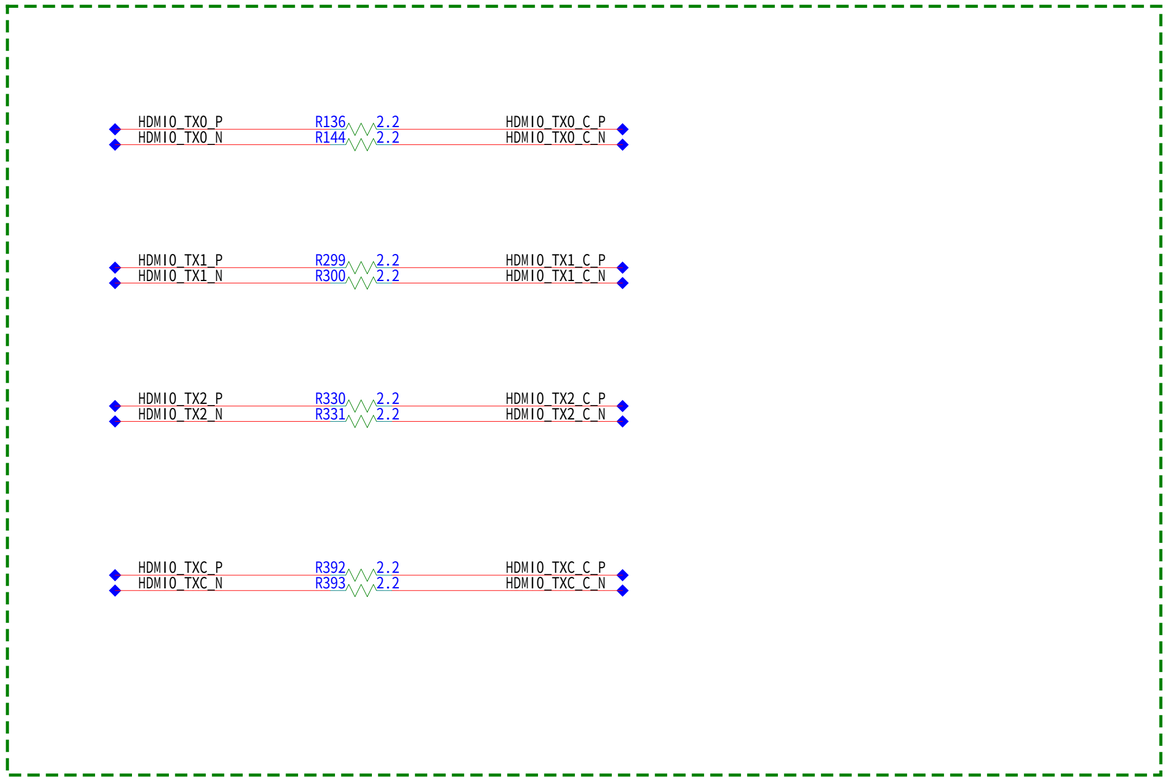
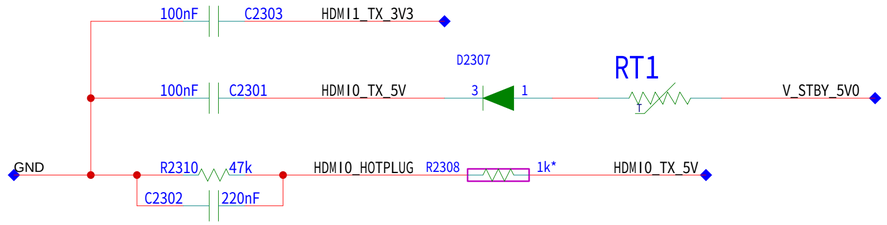
HDMI0 2.0 OUT

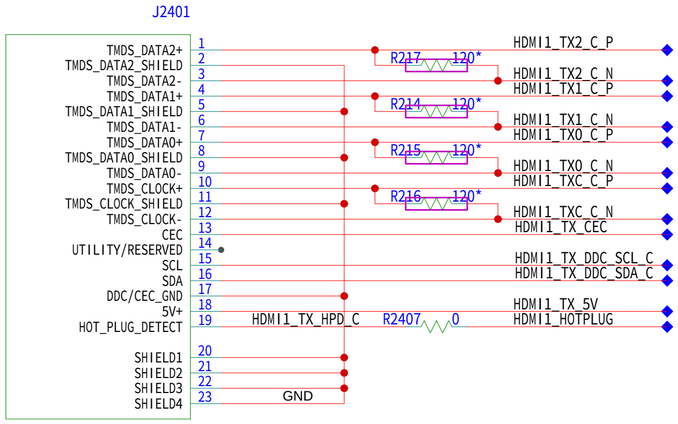

J2301
TMDS_DATA2+ 1
TMDS_DATA2_SHIELD 2
TMDS_DATA2- 3
TMDS_DATA1+ 4
TMDS_DATA1_SHIELD 5
TMDS_DATA1- 6
TMDS_DATA0+ 7
TMDS_DATA0_SHIELD 8
TMDS_DATA0- 9
TMDS_CLOCK+ 10
TMDS_CLOCK_SHIELD 11
TMDS_CLOCK- 12
CEC 13
UTILITY/RESERVED 14
SCL 15
SDA 16
DDC/CEC_GND 17
5V+ 18
HOT_PLUG_DETECT 19
SHIELD1 20
SHIELD2 21
SHIELD3 22
SHIELD4 23
GND
R210 120*
R211 120*
R212 120*
R213 120*
HDMI0_TX2_C_P
HDMI0_TX2_C_N
HDMI0_TX1_C_P
HDMI0_TX1_C_N
HDMI0_TX0_C_P
HDMI0_TX0_C_N
HDMI0_TXC_C_P
HDMI0_TXC_C_N
HDMI0_TX_CEC
HDMI0_TX_DDC_SCL_C
HDMI0_TX_DDC_SDA_C
HDMI0_TX_5V
HDMI0_HOTPLUG
HDMI0_TX_HPD_C
R2309 0

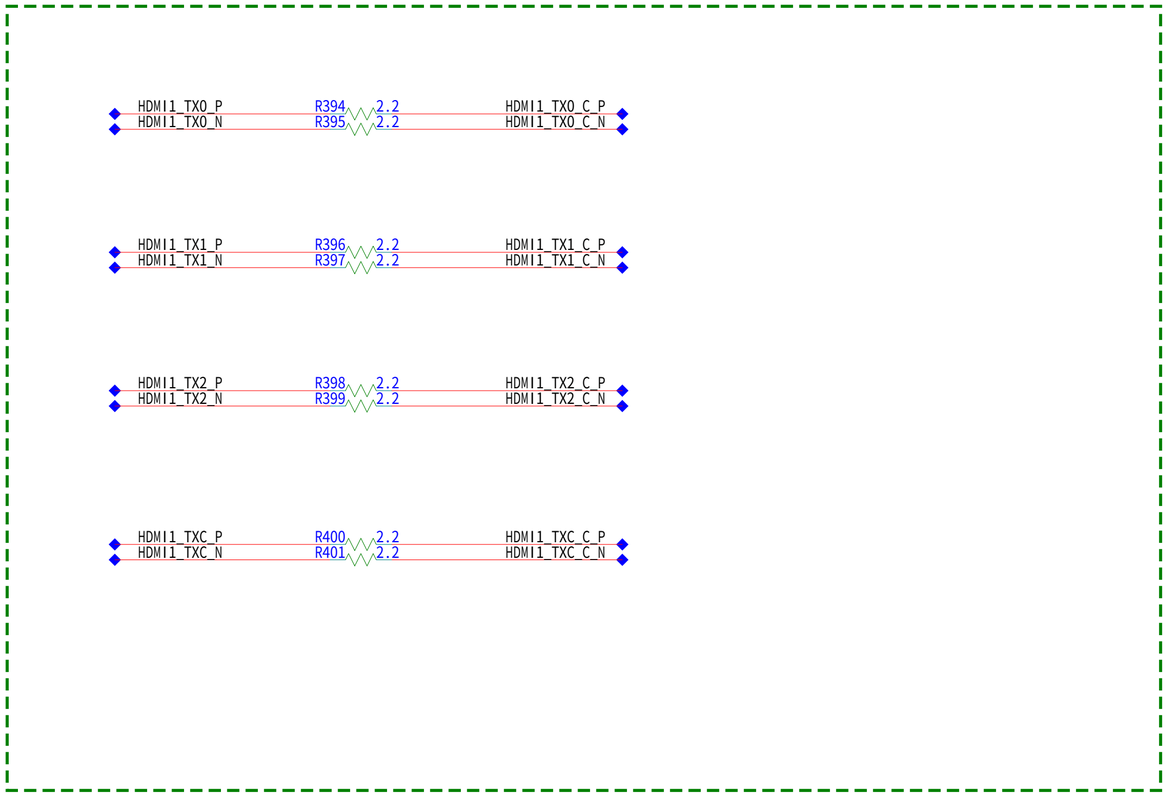

靠近端口侧放置
U13
HDMI0_TX_HPD_C 1
GND 2
HDMI0_TX_CEC 3
6 HDMI0_TX_DDC_SCL_C
5 HDMI0_TX_5V
4 HDMI0_TX_DDC_SDA_C
SRV05-4
D2305
HDMI0_TXC_C_N 1
HDMI0_TXC_C_P 2
GND 3
HDMI0_TX0_C_N 4
HDMI0_TX0_C_P 5
I/O_1
I/O_2
VSS1
I/O_3
I/O_4
NC1 10
NC2 9
VSS2 8
NC3 7
NC4 6
HDMI0_TXC_C_N
HDMI0_TXC_C_P
GND
HDMI0_TX0_C_N
HDMI0_TX0_C_P
D2303
HDMI0_TX1_C_N 1
HDMI0_TX1_C_P 2
GND 3
HDMI0_TX2_C_N 4
HDMI0_TX2_C_P 5
HDMI0_TX1_C_N
HDMI0_TX1_C_P
GND
HDMI0_TX2_C_N
HDMI0_TX2_C_P
HDMI0_TX_5V
HDMI1_TX_3V3
R2317 4.7k
R2307 4.7k
R2301 27k
HDMI0_SCL
HDMI0_SDA
HDMI0_CEC
R2305 100
R2306 100
R2302 100
HDMI0_TX_DDC_SCL_C
HDMI0_TX_DDC_SDA_C
HDMI0_TX_CEC
ESD


HDMI0_TX0_P R136 2.2 HDMI0_TX0_C_P
HDMI0_TX0_N R144 2.2 HDMI0_TX0_C_N
HDMI0_TX1_P R299 2.2 HDMI0_TX1_C_P
HDMI0_TX1_N R300 2.2 HDMI0_TX1_C_N
HDMI0_TX2_P R330 2.2 HDMI0_TX2_C_P
HDMI0_TX2_N R331 2.2 HDMI0_TX2_C_N
HDMI0_TXC_P R392 2.2 HDMI0_TXC_C_P
HDMI0_TXC_N R393 2.2 HDMI0_TXC_C_N

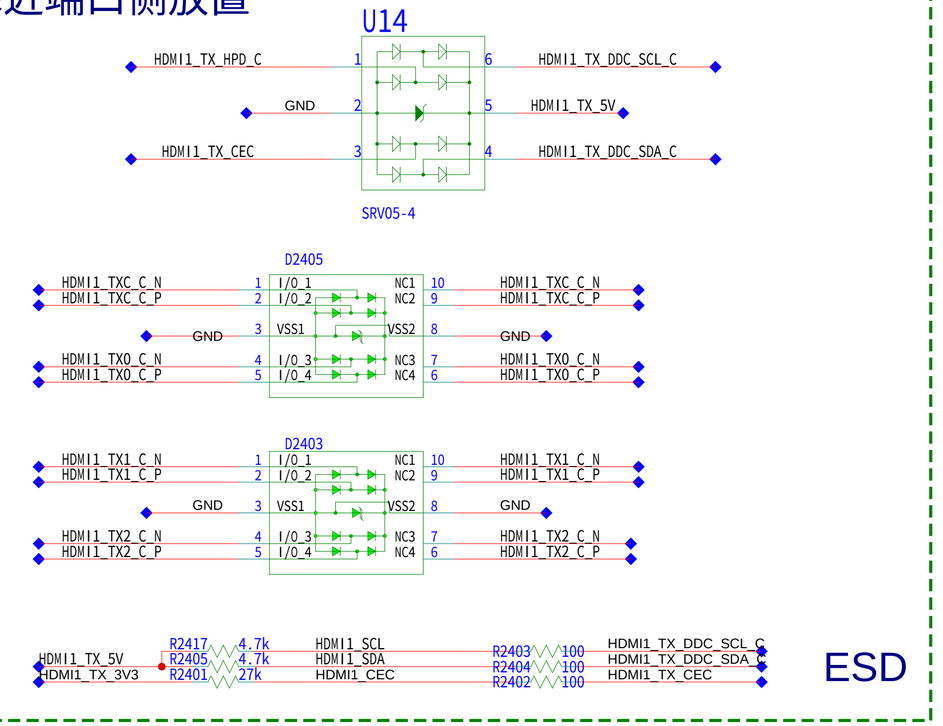

100nF C2303 HDMI1_TX_3V3
D2307
RT1
100nF C2301 HDMI0_TX_5V
3 1
V_STBY_5V0
GND
R2310 47k
HDMI0_HOTPLUG
R2308 1k*
HDMI0_TX_5V
C2302 220nF

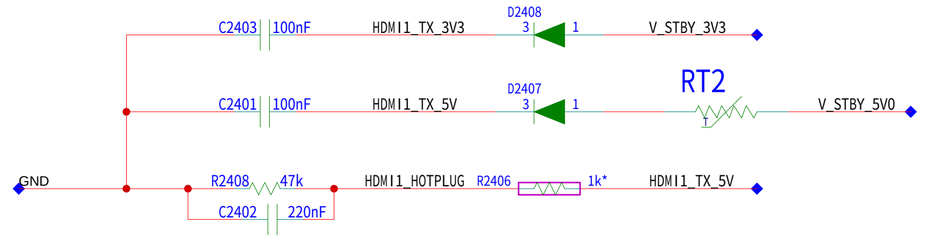
HDMI1 2.0 OUT





靠近端口侧放置





音频接口

AC_MICBIAS0 R2503 0 AC_MICBIAS0_L
R2504 0 AC_MICBIAS0_R
AC_MICBIAS0_L R2501 1.1k
1.1k R2506 AC_MICBIAS0_R
R2505 2.2k* LB2501 V_STBY_3V3
J2501
C2506 100nF
C2505 2.2uF
R2502 1.1k
R2507 1.1k
C2508 2.2uF
C2507 100nF
AGND_AUDIO
AGND_AUDIO SG1 GND
1LB2502
1LB2503
AC_IN_R
AC_IN_L
M1
LB2504
AGND_AUDIO
Audio in
C2502 1nF
C2501 1nF
C2504 15pF
C2503 15pF
R2508 100k*
R2509 100k*
AGND_AUDIO
D2502
D2501
Audio out
V_STBY_3V3 1LB2506 R2526 2.2k*
J2502
AC_HPOUT_R R2525 0
AC_HPOUT_L R2524 0
C2526 27pF
1LB2507
1LB2508
C2527 27pF
C2528 27pF
C2530 1nF
C2531 1nF
C2529 1nF
C2532 1nF
LB2509
M1
AGND_AUDIO
D2504
D2503
R2521 10k
C2525 100pF
AGND_AUDIO
U4
AC_OUT_L C2524 10uF R2522 2.49k
R2523 1k
REFER_2V5 R2518 100k
AGND_AUDIO C2523 1nF
IN- IN+ V- V+ OUT
C2522 10uF R2519 560 AC_HPOUT_L
R2520 4.7k
C2521 1nF
AGND_AUDIO
V_VCC_AUDIO_5V0
C2515 100nF
AGND_AUDIO
V_STBY_5V0
LB2505
C2514 1uF
C2513 100nF
GND
C2512 1uF
C2511 100nF
AGND_AUDIO
R2511 100k
V_VCC_AUDIO_5V0
R2510 100k
C2509 1uF
C2510 100nF
AGND_AUDIO
REFER_2V5
R2514 10k
C2516 100pF
AGND_AUDIO
U4
AC_OUT_R C2517 10uF R2513 2.49k
R2512 1k
REFER_2V5 R2517 100k
AGND_AUDIO C2519 1nF
IN- IN+ V- V+ OUT
C2518 10uF R2516 560 AC_HPOUT_R
R2515 4.7k
C2520 1nF
AGND_AUDIO
V_VCC_AUDIO_5V0

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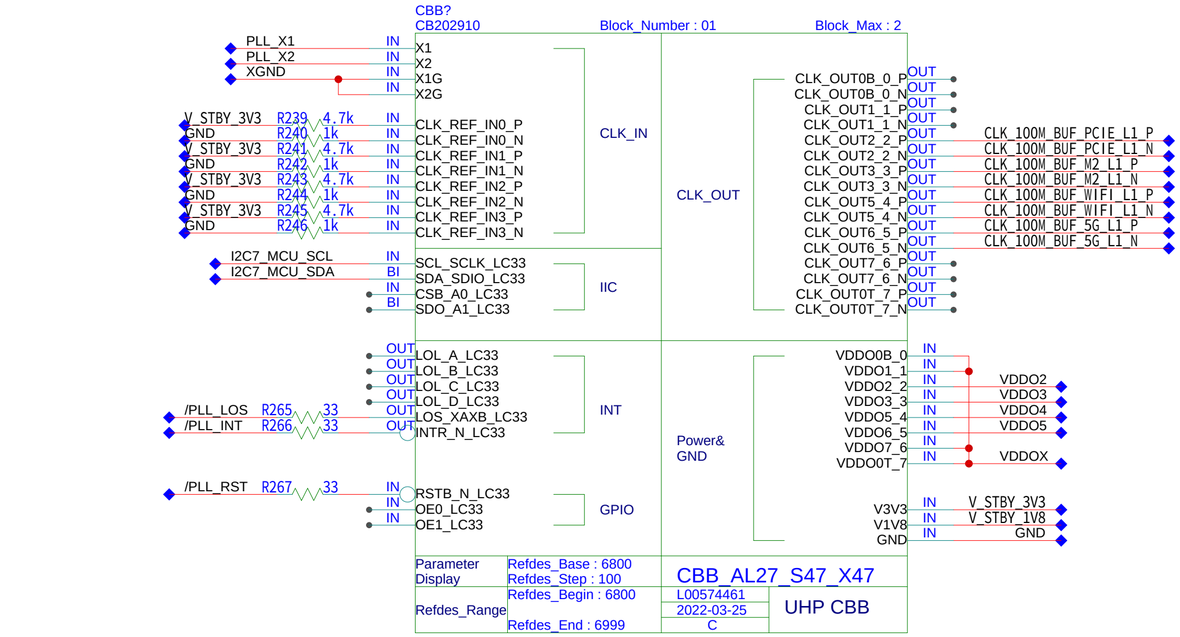
CLOCK



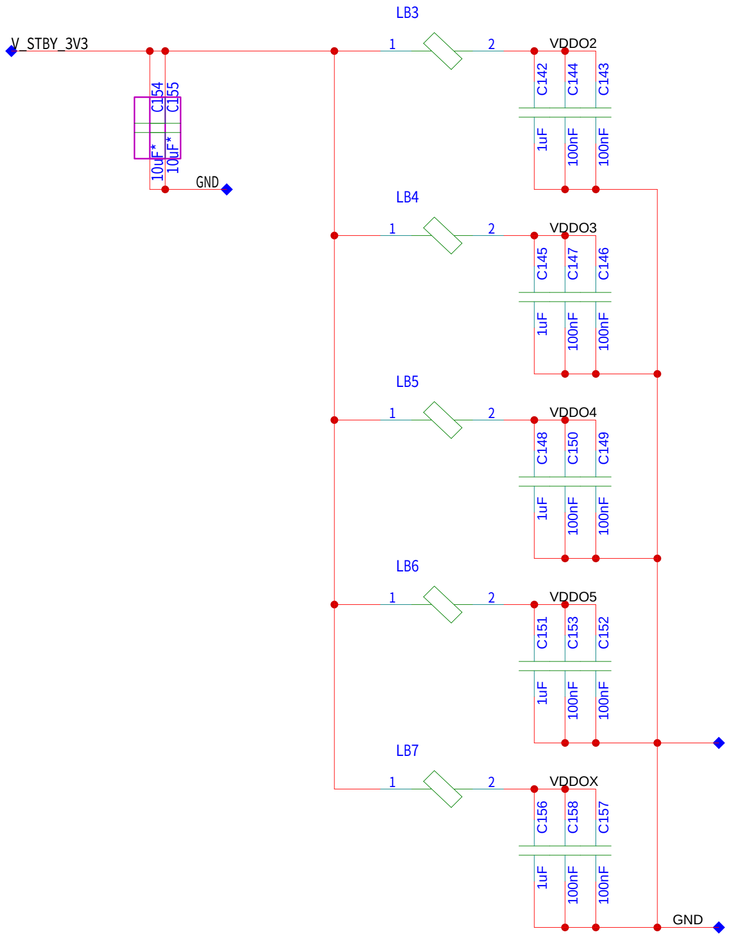
电阻靠近CLOCK DRIVER放置

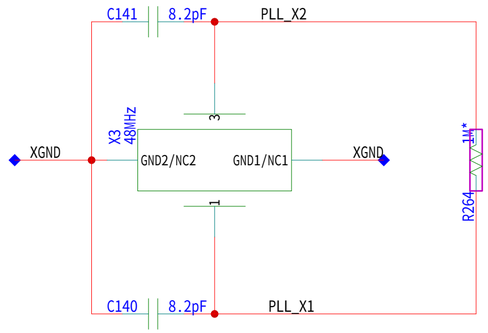
CLK_100M_BUF_PCIE_L1_P R2616 33 CLK_100M_PCIE_L2_P — C2621 100nF SERDES_CLK0_P
CLK_100M_BUF_PCIE_L1_N R2615 33 CLK_100M_PCIE_L2_N — C2622 100nF SERDES_CLK0_N
0: HCSL -> HCSL
R2627 49.9 GND
R2628 49.9 GND

CLK_100M_BUF_M2_L1_P R2618 33 CLK_100M_M2_L2_P — C2623 100nF* CLK_100M_BUF_M2_P
CLK_100M_BUF_M2_L1_N R2617 33 CLK_100M_M2_L2_N — C2624 100nF* CLK_100M_BUF_M2_N
1: HCSL -> HCSL
R2625 49.9 GND
R2626 49.9 GND

CLK_100M_BUF_WIFI_L1_P R2613 33 CLK_100M_WIFI_L2_P — C2620 100nF CLK_100M_BUF_WIFI_P
CLK_100M_BUF_WIFI_L1_N R2614 33 CLK_100M_WIFI_L2_N — C2619 100nF CLK_100M_BUF_WIFI_N
2: HCSL -> HCSL
R2623 49.9 GND
R2624 49.9 GND

CLK_100M_BUF_5G_L1_P R2642 33 CLK_100M_5G_L2_P — C2634 100nF CLK_100M_BUF_5G_P
CLK_100M_BUF_5G_L1_N R2643 33 CLK_100M_5G_L2_N — C2633 100nF CLK_100M_BUF_5G_N
3: HCSL -> HCSL
R2647 49.9 GND
R2646 49.9 GND





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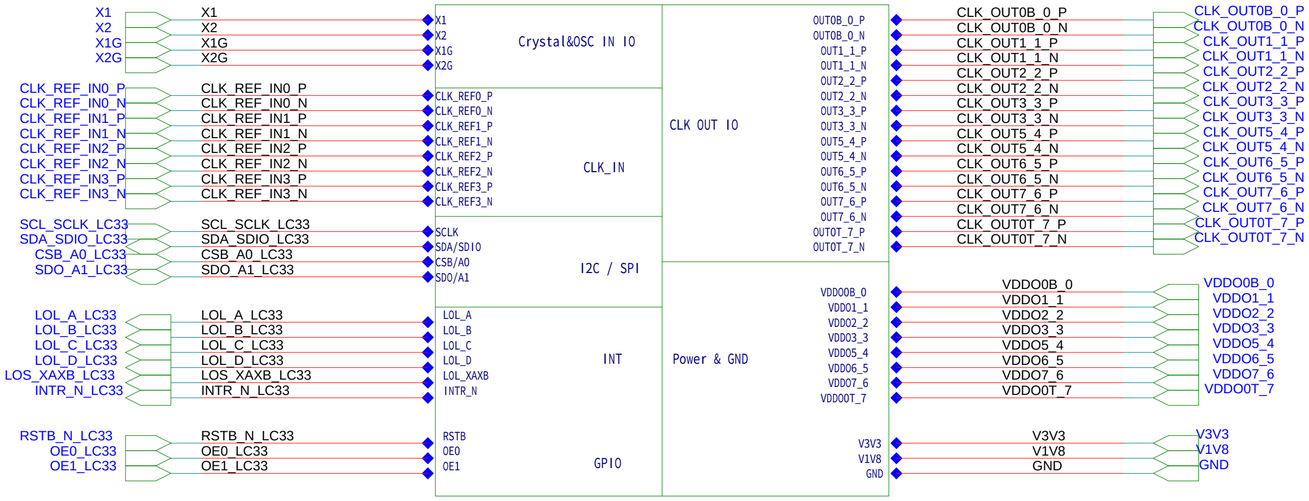
For details about the peripheral circuits of the CBB,see the white block diagram.

NOTE: Huawei internal CBB. Do not discuss with external suppliers or take screenshots. ! ! !

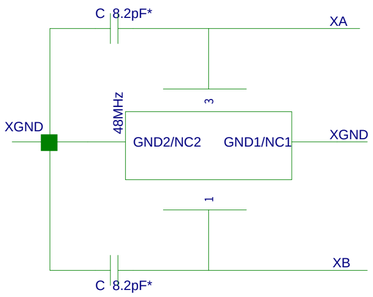


Output Note：

X47：When the OUT1 pin is used for output, if the output clock frequency ranges from 50 MHz to 90 MHz, the output clock cannot be used as a high-performance clock (HI30/HI60, RMS jitter less than 300 fs) but can be used as a common performance clock (jitter less than 1 ps). There is no restriction on other frequencies.

L27/S47/X47:
1.Generally, it is not recommended to output single-ended clock signals.If different reference sources are used or the output frequency is not multipled, the single-ended clock output pin must be separated from the differential clock output pin by at least two channels. Otherwise, the output clock performance of the differential pin will be affected (not meeting the H30/H60 requirements). The two differential outputs corresponding to different reference source inputs must be separated by one channel.
2. Intra-frequency clocks output by the same loop or clocks with frequency multiplication relationships can be discharged without interval output pins.
3. If the same clock source is traced for the same clock output by different loops or the clock with frequency multiplication relationship, the output pins do not need to be spaced.

48 MHz crystal is recommended.

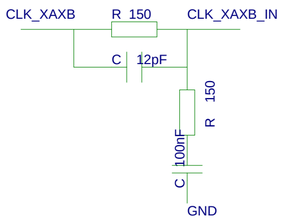


Crystal-compatible crystal oscillator circuit:

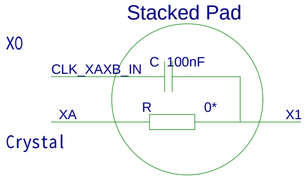
Whether the crystal oscillator circuit is reserved depends on product requirements.

Crystal-compatible crystal oscillator circuit:

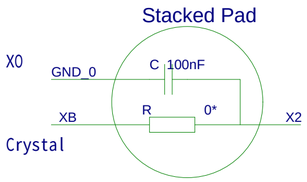
XO Input



Stacked Pad

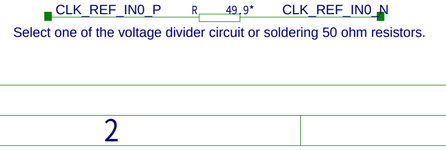


Stacked Pad

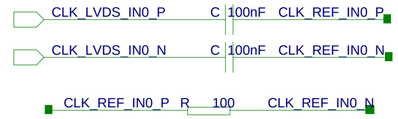


REF_IN:Reference Circuit

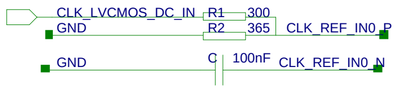
Option1：AC Coupled Differential LVPECL



Option2：AC Couple Differential LVDS/LVPECL



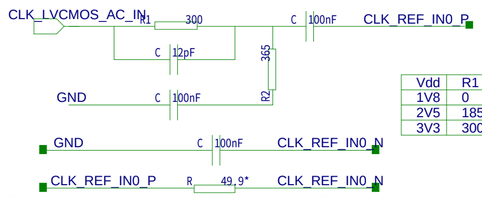
Option3：Pulsed CMOS DC Coupled Signle Ended



Vdd	R1	R2
1V8	0	Null
2V5	185	475
3V3	300	365

When LVCMOS DC Coupling,please select the appropriate resistance to be compatible with the requirements of the co-coding chip for the signle-ended DC input
AL27 LVCOMS DC Vih higher than 0.8V S47 LVCOMS DC Vih higher than 0.8V
X47 LVCOMS DC Vih higher than 0.9V

Option4：Pulsed CMOS AC Coupled Signle Ended

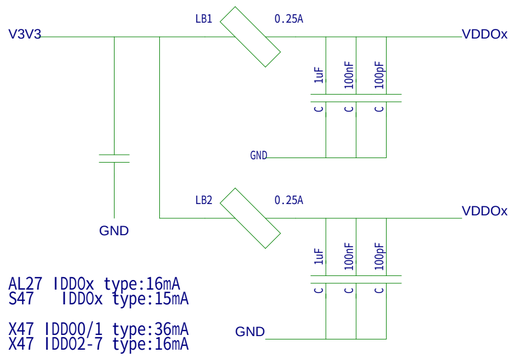


Vdd	R1	R2
1V8	0	Null
2V5	185	475
3V3	300	365

Select one of the voltage divider circuit or soldering 50 ohm resistors.

VDDOx:Reference Filter Circuit

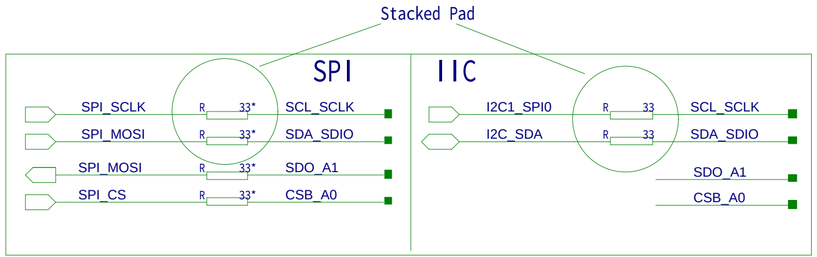
Each product designs its own VDDOx circuiu as needed



AL27 IDDOx type:16mA
S47 IDDOx type:15mA

X47 IDDO0/1 type:36mA
X47 IDDO2-7 type:16mA

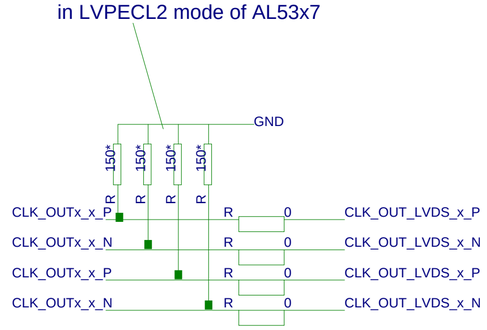
Stacked Pad



CLK_OUT:Reference Circuit

Option for Diff Output

The 150 ohm resistor is only used in LVPECL2 mode of AL53x7



NOTE:It is recommended to use LVDS output string 0 ohm resistor

CLOCK CBB -1

SHEET 1 OF 3

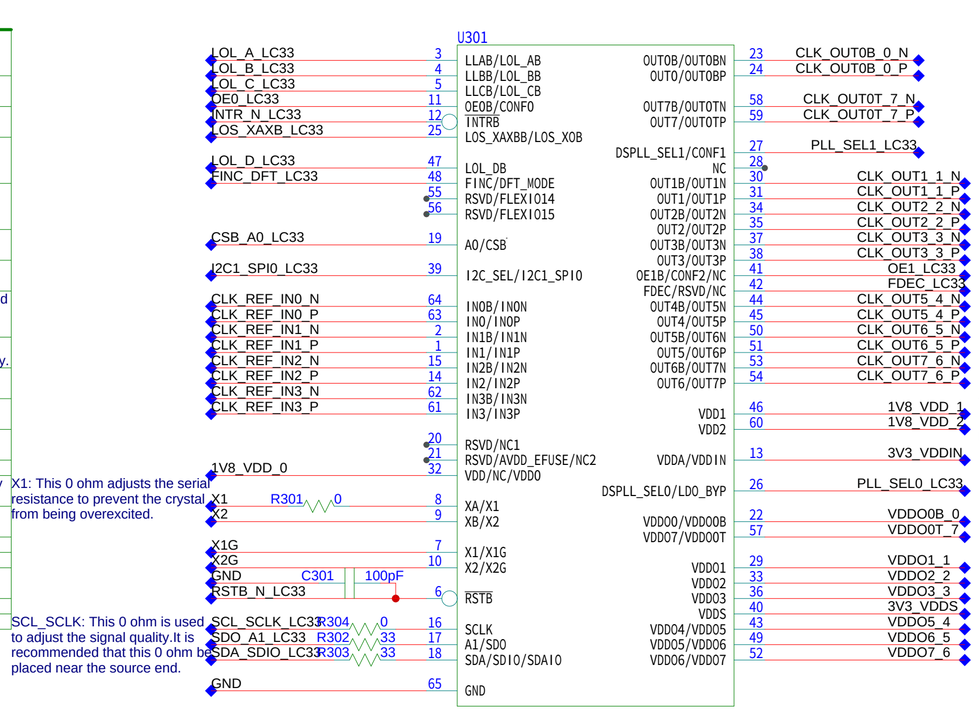
CLOCK CBB -2

NOTE: Huawei internal CBB. Do not discuss with external suppliers or take screenshots. ！ ！ ！

Compatible with S47 and AL27 and X47

PIN	S47	AL27	X47
3	LOL_A	LOL_A	LOL_A
4	LOL_B	LOL_B	LOL_B
5	LOL_C	LOL_C	LOL_C
11	OE0b	OE0b	OE0b
12	INTR	INTR	INTR
25	LOS_XAXB	LOS_XOB	LOS_XAXB
47	LOL_D	LOL_D	LOL_D
48	FINC	FINC	FINC
55	RSVD	FLEXIO14	RSVD
56	RSVD	FLEXIO15	RSVD
19	CSb/A0	CSb	CSb/A0
39	I2C_SEL	I2C1_SPI0	I2C_SEL
64	IN0b	IN0N	IN0b
63	IN0	IN0P	IN0
2	IN1b	IN1N	IN1b
1	IN1	IN1P	IN1
15	IN2b	IN2N	IN2b
14	IN2	IN2P	IN2
62	IN3b	IN3N	IN3b
61	IN3	IN3P	IN3
20	RSVD	NC	RSVD
21	RSVD	NC	RSVD
32	VDD	NC	VDD
8	XA	X1	XA
9	XB	X2	XB
7	X1	X1G	X1
10	X2	X2G	X2
6	RSTb	RSTB	RSTb
16	SCLK	SCLK	SCLK
17	SDO/A1	SDO	SDO/A1
18	SDA/SDIO	SDAIO	SDA/SDIO
65	GND	GND	GND

PIN	Pin Differences
	This pin is not used in normal applications of the three chips and requires pull-down.
11 OE0b	For S47 and L27, this pin controls the output enable of all outputs. For X47, this pin can control all output enable status only after this pin is enabled in the register.
19 CSb/A0	L27 does not support the 3-wire SPI mode.Both X47 and S47 support the 3-wire SPI mode. L27 does not support continuous reading and writing of multiple registers in SPI mode. Both X47 and S47 support this function. L27 does not support continuous writing of multiple registers in IIC mode. Both X47 and S47 support writing
	This pin is the same for the normal application of the three chips.
40 VDDS	The X47 pin has no actual function and can be connected or not. When the chip of other vendors is compatible, the 3V3 power supply must be connected. S47 This pin determines the VIH/VIL level of the FDEC and OE1b. It must be connected to the 3V3 power supply. L27: This pin determines the VIH/VIL level of the FDEC. It must be connected to the 3V3 power supply.
	This pin is not used in normal applications of the three chips and requires pull-down.
41 OE1b	S47: This pin works with OE1a to enable or disable the chip output.
NC	L27: This pin is not used. For X47, this pin can control all output enable status only after this pin is enabled in the register.
55 RSVD FLEX	This pin is not used when the three chips are normally used. The pin is pulled up or floated. For S47 and X47, this pin has no function. For L27, this pin can be used as a FLEX pin.
56 RSVD FLEX	This pin is not used when the three chips are normally used. The pin is pulled up or floated. For S47 and X47, this pin has no function. For L27, this pin can be used as a FLEX pin.



X1: This 0 ohm adjusts the serial resistance to prevent the crystal from being overexcited.

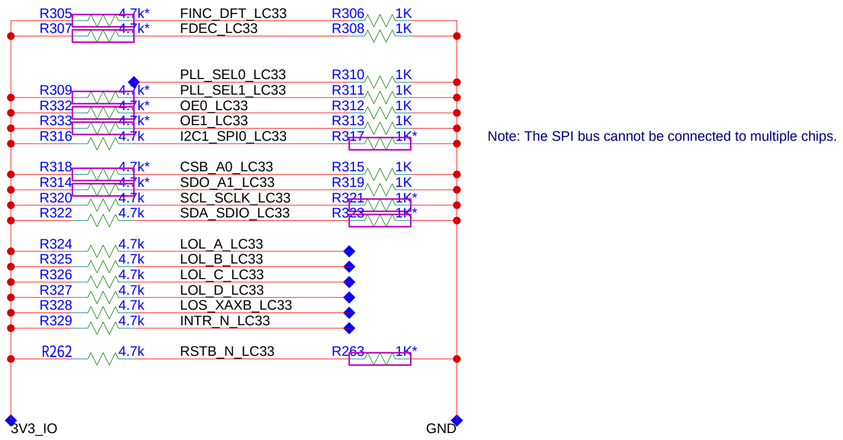
SCL_SCLK: This 0 ohm is used to adjust the signal quality.It is recommended that this 0 ohm be placed near the source end.

The VDD power pins are connected to filter circuits to obtain better phase noise.

PIN	S47	AL27	X47
23	OUT0b	OUT0BN	OUT0b
24	OUT0	OUT0BP	OUT0
58	OUT7b	OUT0TN	OUT7b
59	OUT7	OUT0TP	OUT7
27	DSPLL_SEL1	PLL_SEL1	DSPLL_SEL1
28	NC	NC	NC/RSVD
30	OUT1b	OUT1N	OUT1b
31	OUT1	OUT1P	OUT1
34	OUT2b	OUT2N	OUT2b
35	OUT2	OUT2P	OUT2
37	OUT3b	OUT3N	OUT3b
38	OUT3	OUT3P	OUT3
41	OE1b	NC	OE1b
42	FDEC	FDEC	FDEC
44	OUT4b	OUT5N	OUT4b
45	OUT4	OUT5P	OUT4
50	OUT5b	OUT6N	OUT5b
51	OUT5	OUT6P	OUT5
53	OUT6b	OUT7N	OUT6b
54	OUT6	OUT7P	OUT6
46	VDD	VDD	VDD1
60	VDD	VDD	VDD2
13	VDDA	VDDIN	VDDA
26	DSPLL_SEL_0	PLL_SEL_0	DSPLL_SEL_0
22	VDDO0	VDDOB	VDDO0
57	VDDO7	VDDOT	VDDO7
29	VDDO1	VDDO1	VDDO1
33	VDDO2	VDDO2	VDDO2
36	VDDO3	VDDO3	VDDO3
40	VDDS	VDDS	VDDS
43	VDDO4	VDDO5	VDDO4
49	VDDO5	VDDO6	VDDO5
52	VDDO6	VDDO7	VDDO6

Functions of GPIO pins:

FINC/FDEC	X47/S47/AL27:FINC，Used as frequency up step control in DCO mode X47/S47/AL27:FDEC，Used as frequency down step control in DCO mode
PLL_SEL0/1	X47/S47/AL27:PLL_SEL0 with PLL_SEL1，Loop selection signal for pin control in DCO mode
OE1/OE2	X47/S47/AL27: OE1 works with OE2 to determine all output configurations of the chip.X47/S47/AL27: Pull-down resistors must be connected to the ground. Pull-up resistors cannot be connected or floated.The pull-up resistors in the circuit must be soldered and reserved. Note that the X47 can be used only after the register is configured.
I2C1_SPI0	I2C_SEL=1：IIC mode; I2C_SEL=0 SPI mode Pull-up IIC mode and pull-down SPI mode. The IIC mode is recommended.
A0/A1	A0: used as the A0 address in IIC mode and as the chip select pin in SPI mode. Internal pull-up, floating when not in use. A1: used as the A1 address in IIC mode and as the 4-wire SPI data output pin in SPI mode;
LOL_A/B/C/D	SCLK: SCL in IIC mode and SCLK in SPI mode; SDAIO: SDA in IIC mode; bi-direction data in 3-wire SPI mode; data input in 4-wire SPI mode
SCLK/SDAIO	LOLA: PLLA loop lock status interrupt indication signal. It is recommended that this signal be connected to the logic. LOLB: PLLB loop lock status interrupt indication signal. It is recommended that this signal be connected to the logic. LOLC: PLLC loop lock status interrupt indication signal. It is recommended that this signal be connected to the logic. LOLD: PLLD loop lock status interrupt indication signal. It is recommended that this signal be connected to the logic. LOL_XAXB: LOS interrupt indication signal of the XAXB working clock. It is recommended that this signal be connected to the logic.
INTRb	INTRb: interrupt indication signal. It is recommended that this signal be connected to the logic.
RSTB	Reset signal, active low; The logic must be connected. Before the chip is initialized, reset and deassert the reset.

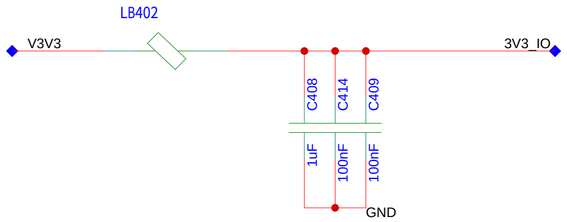


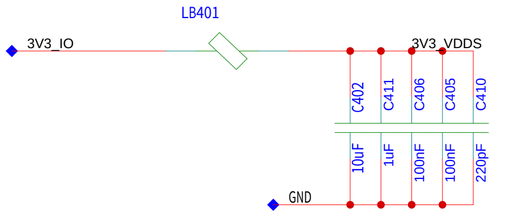
Note: The SPI bus cannot be connected to multiple chips.

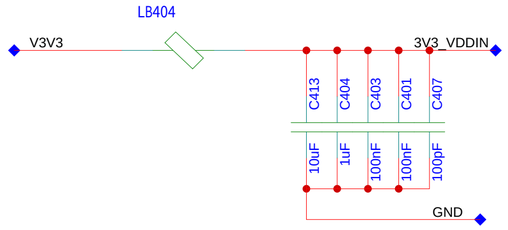
CLOCK CBB -3

Recommended circuit for VDD:

S47/AL27/X47 GPIOs use 3V3 pull-up.

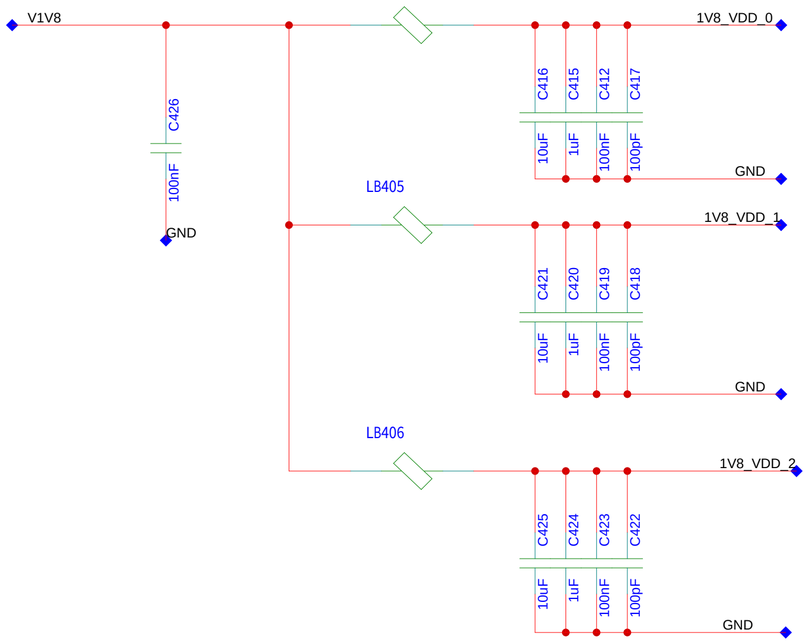






AI27IDDIN type:18mA
S47 IDDIN type:125mA
X47 IDDIN type:70mA

S47/AL27/X47 VDD:1V8



Note: Pins 32, 46, and 60 use independent filter circuits. It is recommended that 100 nF capacitors be placed close to each pin on the PCB.

AL27 IDD type:320mA
S47 IDD type:300mA
X47 IDD type:480mA

EEPROM
U2701
Addr:b1010_000x(0xA0)
TPM
在位信号说明
SPI TPM芯片P2P
国密：41010376/41010376-002
国外：41010291/41010494
可信要求TPM/CPU同步上电
J2701
靠近MXM连接器放置
U2704
Q3
PMOS-GSD
Q2
FETN-GSD
Q4
U17
U2703
Addr: b0100_010x(0x40)
SHEET 27 OF 37

MCU

CBB

EN_MCU_HOT1 R2813 33 GPIO0 加热电阻控制-模组
EN_MCU_HOT2 R2812 33 GPIO1 加热电阻控制-HUB
HEALTHY_LED_MCU_G R2836 33 GPIO2 健康状态正常指示灯
HEALTHY_LED_MCU_R R2834 33 GPIO3 健康状态异常指示灯
POWER_LED_MCU_G R2835 33 GPIO4 电源指示灯绿色
POWER_LED_MCU_R R2832 33 GPIO5 电源指示灯红色
GPIO6
GPIO7
RSV_GPIO_R R2842 33 GPIO8 预留GPIO
/RST_MCU_1911_R R2848 33 GPIO9 MCU复位模组
TAISHAN_POROFF_IN R2846 33 GPIO10 安全上下电输入
TAISHAN_SLEEP_IN_R R2843 33 GPIO11 休眠唤醒输入
UHT_ALARM R2841 33 GPIO12 过温报警信号
FACTORYSET_1911_R R2839 33 GPIO13 恢复模组出厂设置
V_STBY_3V3 R414 4.7k GPIO14
GPIO15
GPIO16
TPM_TYPE R203 33 GPIO17
/PLL_LOS 0 R270 GPIO18
/PLL_INT 0 R268 GPIO19
/PLL_RST 0 R269 GPIO20
GPIO21
GPIO22
TYPE_ID0 0 R125 TYPE_ID0
TYPE_ID1 0 R126 TYPE_ID1
/FACTORYSET_MCU R2833 0 BREAKER_STATE0 恢复出厂设置按键
/POWER_BTN_MCU R2827 0 BREAKER_STATE1 电源按键
/RST_BTN_MCU R2831 0 BREAKER_STATE2 复位按键
SYS_RST_OUT_R R2847 0 BREAKER_STATE3 模组复位输出信号
TAISHAN_POROFF_OUT R2845 0 BREAKER_STATE4 安全上下电输出
TAISHAN_SLEEP_OUT_R R2844 0 BREAKER_STATE5 休眠唤醒输出
1911_OS_OK_R R2837 0 BREAKER_STATE6 OS启动OK
HOT_RST_FAULT_R R2838 0 BREAKER_STATE7 令复位输出
1911_HBOOT_OK_R R2840 0 BREAKER_STATE8 Hboot启动OK
/PG_24711_POWER BREAKER_STATE9
BREAKER_STATE10
BREAKER_STATE11
BREAKER_STATE13
BREAKER_STATE14
INT_MCU_1911_R R66 0 EX_INT
INT_1911_MCU_R R65 0
SENSE_VIN_12V0 AIN0
SENSE_VCC_5V0 AIN1
SENSE_VCC_3V3 AIN2
SENSE_LTE_3V8 AIN3
SENSE_LTE_3V3 AIN8
VRT_DET AIN9
SENSE_TEC_OUT AIN10
SENSE_VBAT_3V0 AIN11

BOARD_ID0 R2853 0 BOARD_ID0
BOARD_ID1 R2854 0 BOARD_ID1
BOARD_ID2 R2855 0 BOARD_ID2
BOARD_ID3 R2856 0 BOARD_ID3
BOARD_ID4 R2857 0 BOARD_ID4
BOARD_ID5 R2858 0 BOARD_ID5
BOARD_ID6 R2859 0 BOARD_ID6
BOARD_ID7 R2860 0 BOARD_ID7
PCB_ID0 R2861 0 PCB_ID0
PCB_ID1 R2862 0 PCB_ID1
PCB_ID2 R2863 0 PCB_ID2
BOM_ID0 R2864 0 BOM_ID0
BOM_ID1 R2865 0 BOM_ID1
BOM_ID2 R2866 0 BOM_ID2
SCL0 R2869 0 I2C0_MCU_SCL
SDA0 R2870 0 I2C0_MCU_SDA master slave：TPA626
SCL1 R2871 33 I2C6_SCL
SDA1 R2868 33 I2C6_SDA slave master：模组
SCL2 R2867 33 I2CS_SCL
SDA2 R2872 33 I2CS_SDA master slave：模组
SCL3 R2874 0 I2C3_MCU_SCL
SDA3 R2873 0 I2C3_MCU_SDA master slave：三路温感
SCL4 R120 0 I2C4_MCU_SCL
SDA4 R123 0 I2C4_MCU_SDA master slave：TEC_PCA9555
SCL7 R271 0 I2C7_MCU_SCL
SDA7 R272 0 I2C7_MCU_SDA master slave：CLK_PLL
UART_UPLNK_TX1 R2879 33 UART1_RX_R
UART_UPLNK_RX1 UART1_TX_R
MCU_SWDIO MCU1_SWDIO
MCU_SWCLK MCU1_SWCLK
SPI_MCU_CS R2876 33 SPI_MCU_CS
SPI_MCU_MISO SPI_MCU_MISO
SPI_MCU_MOSI R2875 33 SPI_MCU_MOSI
SPI_MCU_CLK R2878 33 SPI_MCU_CLK
DEBUG_TX MCU2_SWDIO Z型号的debug串口
DEBUG_RX MCU2_SWCLK H型号的debug/SWDIO复用管脚
UART2_TX UART_MCU_DEBUG
UART2_RX UART_DEBUG_MCU
VREF_ADC MCU_VREF
MCU_RST_N C2810 100nF GND
3V3 V_STBY_3V3
GND GND
1V8 R2826 0* V_STBY_1V8
4.7k R2828 GND
BOOT0 MCU_BOOT0 TP6
4.7k* R2829 V_STBY_3V3
C2809 10uF C2808 10uF C2807 10uF C2806 10uF C2805 10uF GND

V_STBY_3V3
R25 4.7k MCU1_SWCLK
R26 4.7k MCU1_SWDIO
R227 4.7k UART_DEBUG_MCU
R228 4.7k UART_MCU_DEBUG
R33 4.7k UART1_RX_R
R34 4.7k UART1_TX_R
R28 4.7k I2C0_MCU_SCL
R27 4.7k I2C0_MCU_SDA
R37 4.7k I2C3_MCU_SCL
R38 4.7k I2C3_MCU_SDA
R96 4.7k I2CS_SCL
R97 4.7k I2CS_SDA
R98 4.7k I2C6_SCL
R99 4.7k I2C6_SDA
R35 4.7k I2C4_MCU_SCL
R36 4.7k I2C4_MCU_SDA

U2804 Temp sensor 0
I2C3_MCU_SDA R2881 33 SDA V+/VDD/VCC V_STBY_3V3 C2812 100nF GND
I2C3_MCU_SCL R2882 33 SCL A0 LM75_INLET0_A0
ALERT/OS/ALERT/INT/OS A1 LM75_INLET0_A1
GND GND A2 LM75_INLET0_A2
Addr:b1001_001x(0x92)
R2894 1k* LM75_INLET0_A0 R2891 4.7k V_STBY_3V3
R2896 1k LM75_INLET0_A1 R2893 4.7k*
GND R2895 1k LM75_INLET0_A2 R2892 4.7k*

U2803 Temp sensor 1
I2C3_MCU_SDA R2884 33 SDA V+/VDD/VCC V_STBY_3V3 C2813 100nF GND
I2C3_MCU_SCL R2883 33 SCL A0 LM75_INLET1_A0
ALERT/OS/ALERT/INT/OS A1 LM75_INLET1_A1
GND GND A2 LM75_INLET1_A2
Addr:b1001_010x(0x94)
R23 4.7k LM75_INLET1_A0 R24 1k* V_STBY_3V3
R2899 1k* LM75_INLET1_A1 R21 4.7k
GND R62 1k LM75_INLET1_A2 R22 4.7k*

U2805 Temp sensor 2
I2C3_MCU_SDA R2886 33 SDA V+/VDD/VCC V_STBY_3V3 C2811 100nF GND
I2C3_MCU_SCL R2885 33 SCL A0 LM75_INLET2_A0
ALERT/OS/ALERT/INT/OS A1 LM75_INLET2_A1
GND GND A2 LM75_INLET2_A2
Addr:b1001_011x(0x96)
R2890 1k* LM75_INLET2_A0 R2887 4.7k V_STBY_3V3
R2898 1k* LM75_INLET2_A1 R2889 4.7k
GND R2897 1k LM75_INLET2_A2 R2888 4.7k*

SPI FLASH U2801
SPI_MCU_MOSI 5 SI/SIO0/IO0 CS 1 R2805 4.7k V_STBY_3V3
SPI_MCU_MISO 33 R2806 2 SO/SIO1/IO1 SCLK 6 SPI_MCU_CS
V_STBY_3V3 4.7k R2830 3 WP/SIO2/IO2 VCC 8 SPI_MCU_CLK
4.7k R2804 7 RESET/SIO3/HOLD/IO3 GND/VSS 4 V_STBY_3V3 35mA C2801 100nF GND

V_STBY_3V3 R2803 4.7k* SPI_MCU_MISO
R2809 4.7k* SPI_MCU_MOSI
R2810 4.7k* SPI_MCU_CLK

V_TEC_OUT R2823 20k SENSE_TEC_OUT 0.83V R2822 10k GND
V_STBY_3V3 R2818 10k SENSE_VCC_3V3 1.35V R2819 10k GND
V_STBY_5V0 R2817 20k SENSE_VCC_5V0 1.6V R2816 10k GND
V_LTE_3V8 R2820 10k SENSE_LTE_3V8 1.9V R2821 10k GND
V_STBY_12V0 R2814 150k SENSE_VIN_12V0 2V R2815 30k GND
V_LTE_3V3 R2825 10k SENSE_LTE_3V3 1.65V R2824 10k GND

MCU_VREF 2.5v 靠近MCU放置 R2811 200 LB2801 V_STBY_3V3
1uF C2802 100nF C2803 U2802 K NC 100nF C2804
GND A GND

MCU1_SWDIO R2801 33 TP1
MCU1_SWCLK R2802 33 TP2
0 R225 0 R226
MCU2_SWDIO R2808 33 TP23
MCU2_SWCLK R2807 33 TP24
GND TP4
UART_MCU_DEBUG R29 33 TP3
UART_DEBUG_MCU R76 33 TP5

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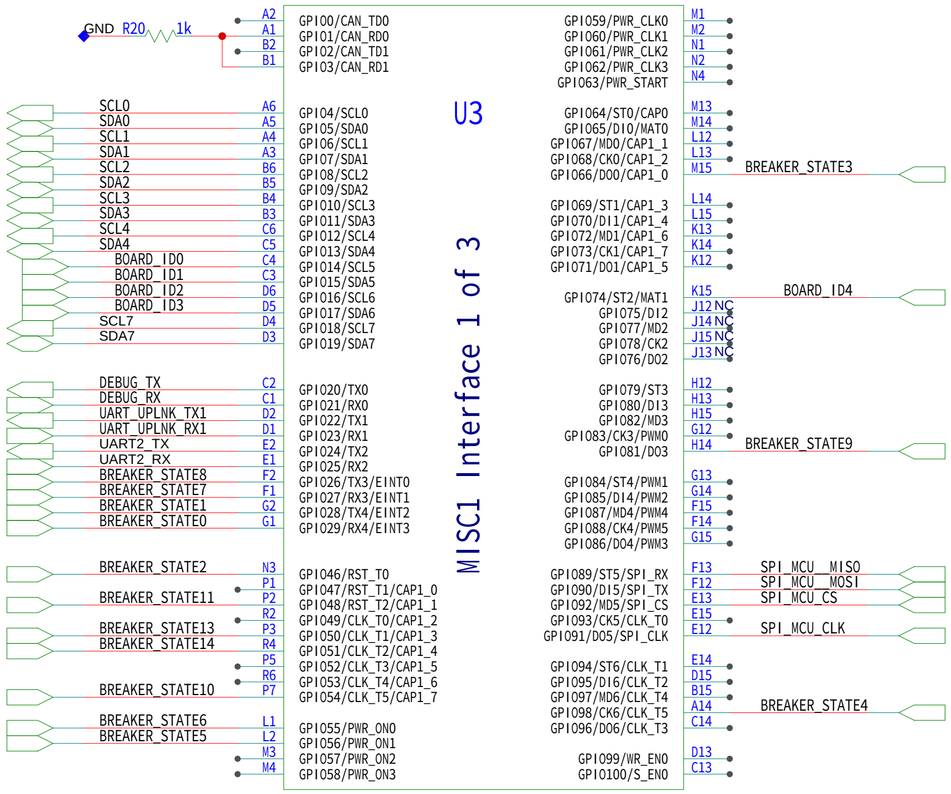
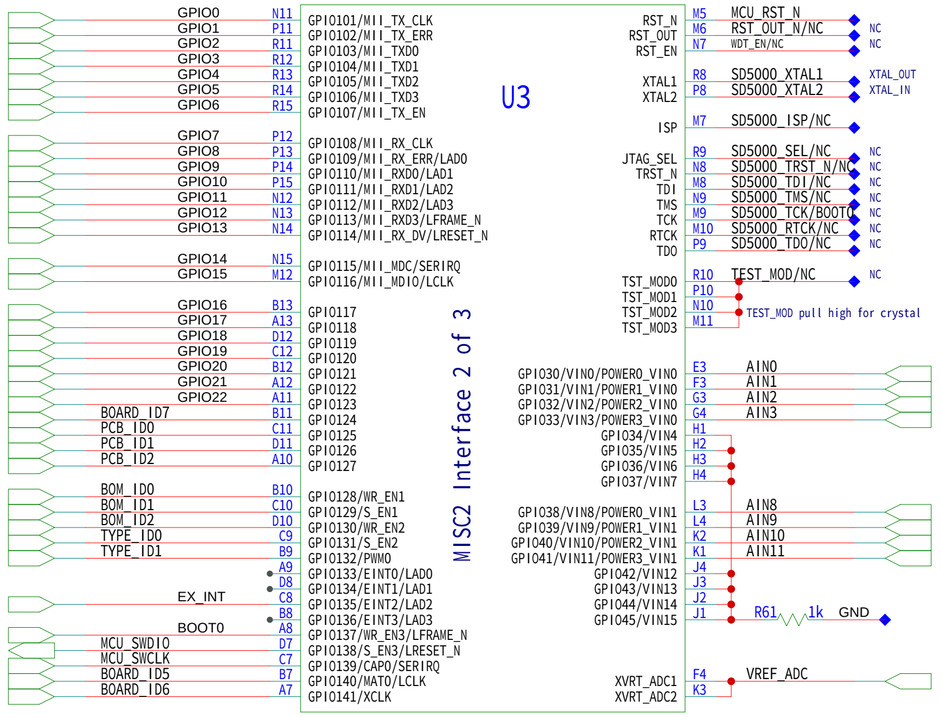
MCU CBB -1

MCU CBB电路

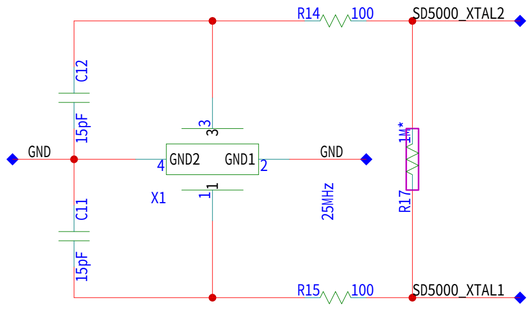
SHEET 1 OF 3

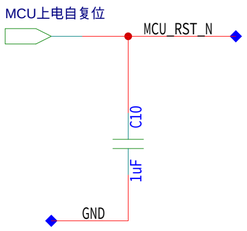
MCU CBB -2

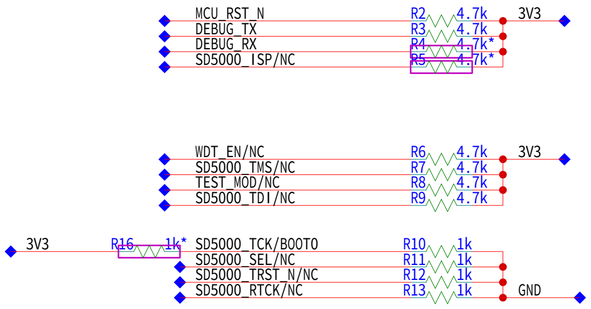




Clock: Crystal

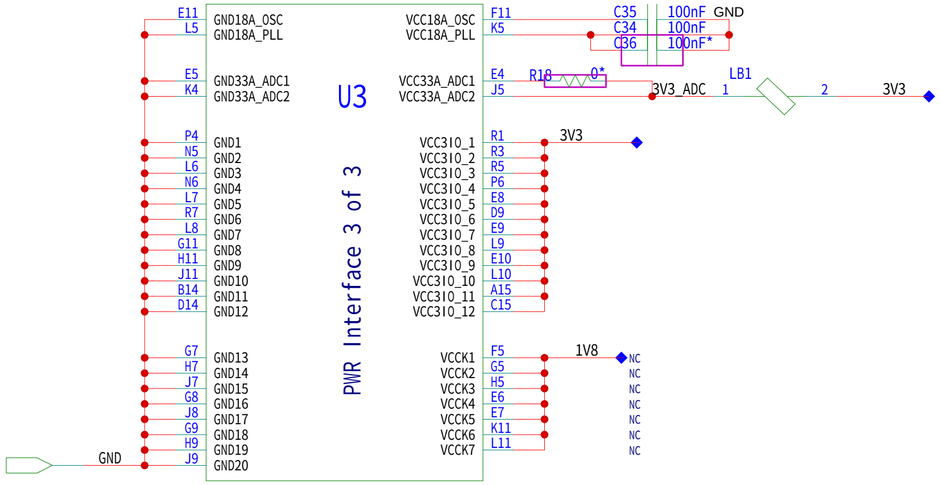


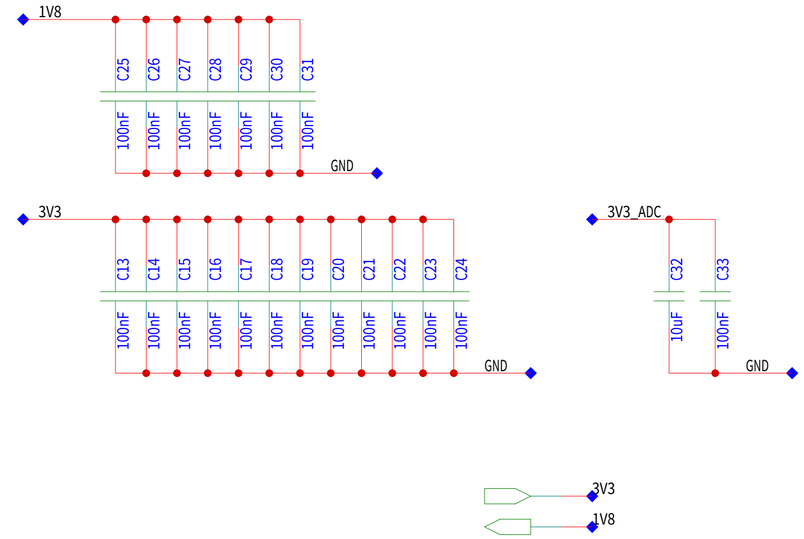




SHEET 2 OF 3

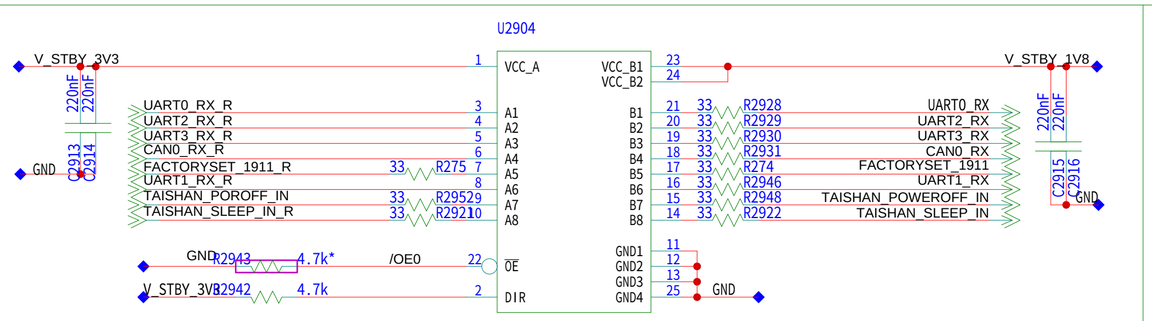
MCU CBB -3

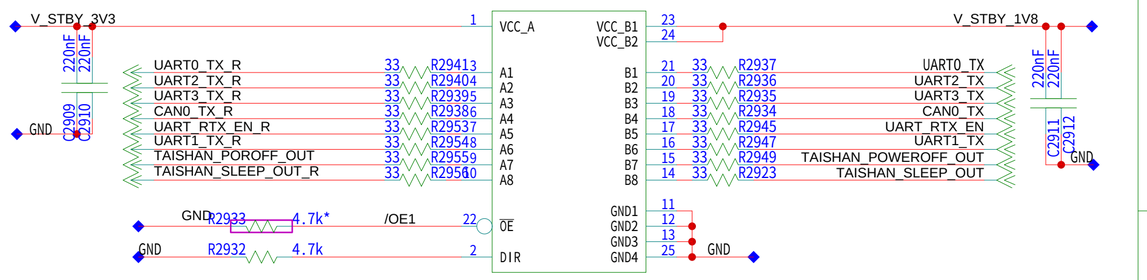


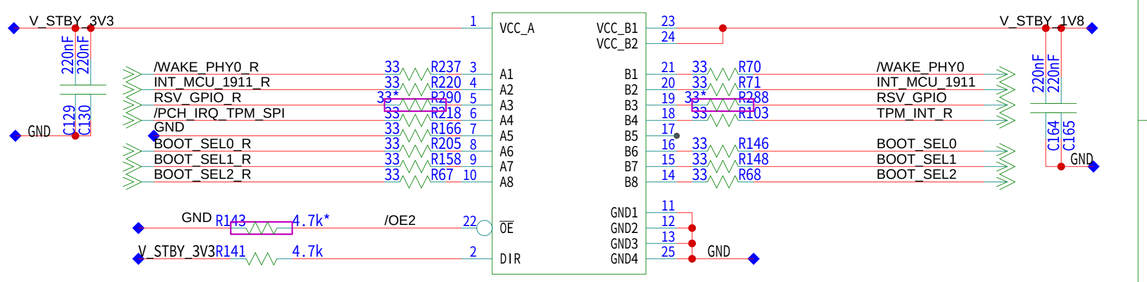


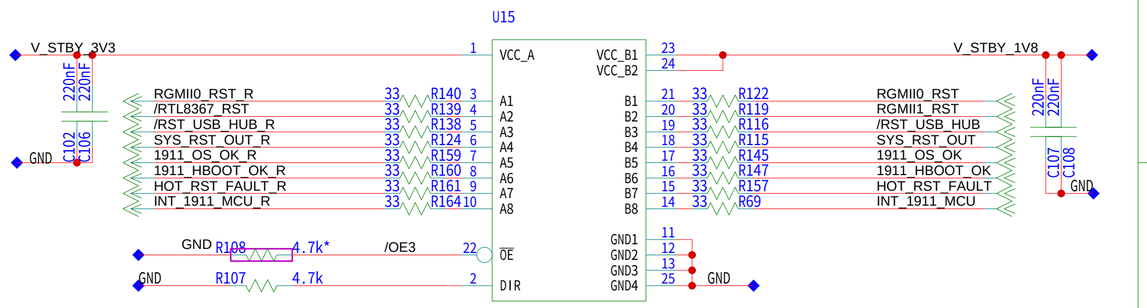
SHEET 3 OF 3

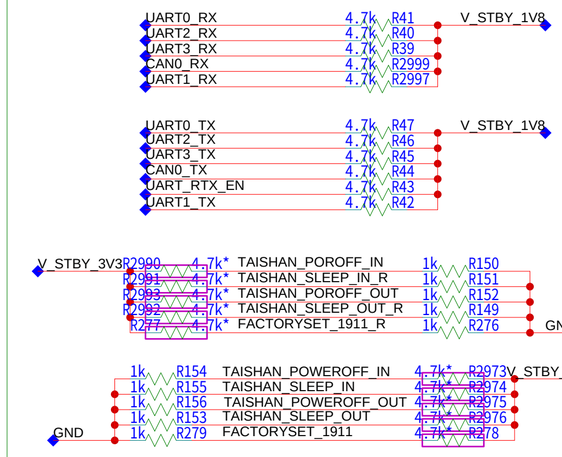
Level Shift

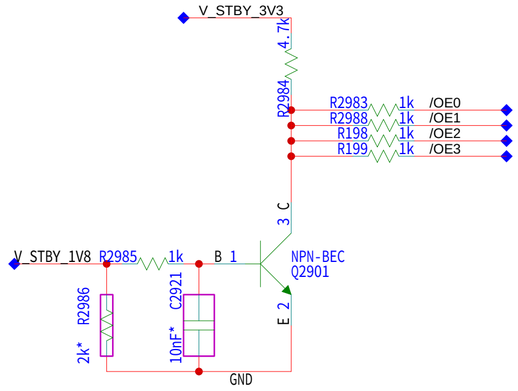


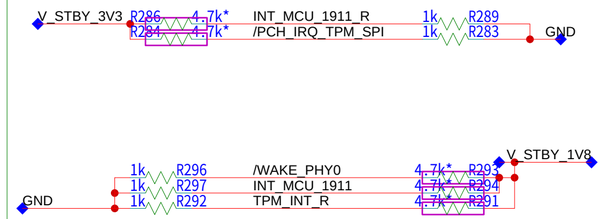


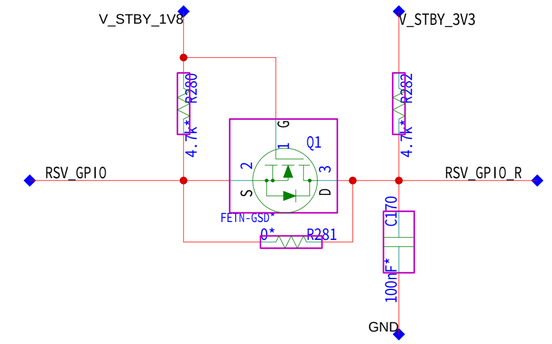


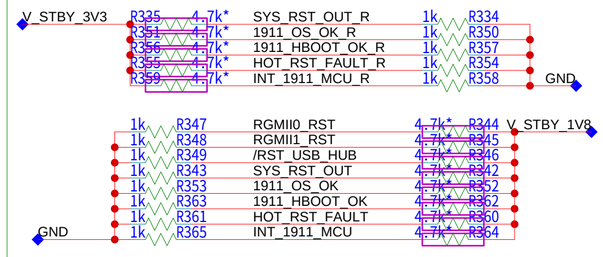


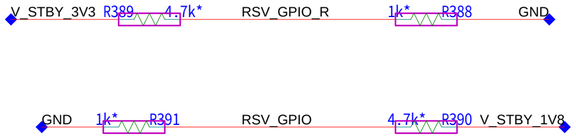






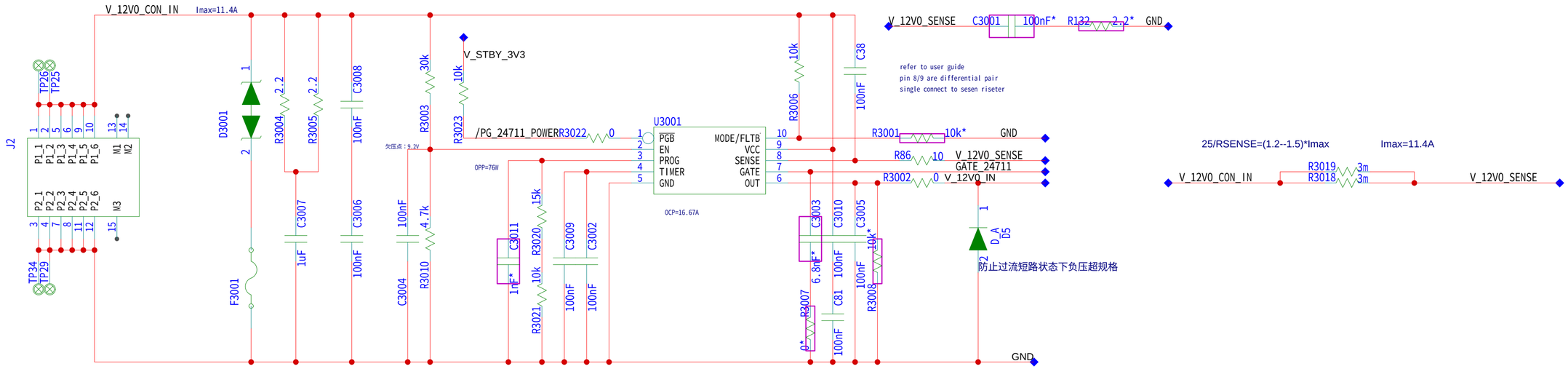


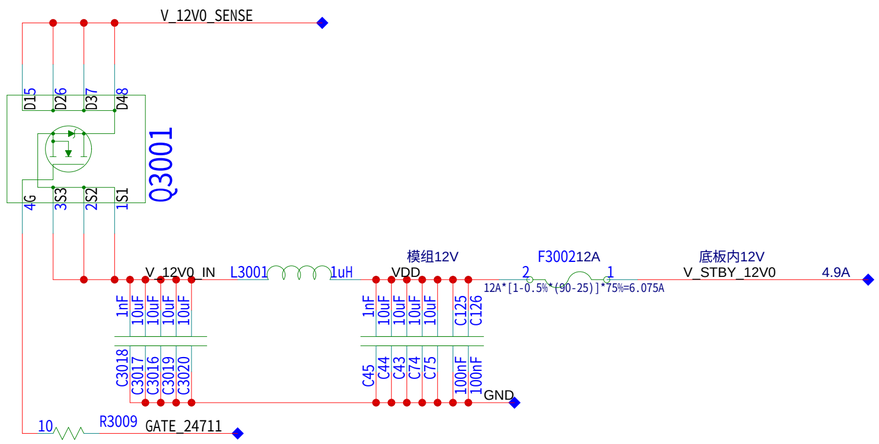


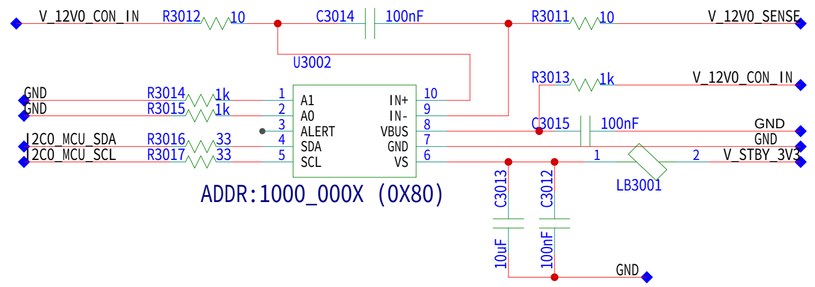


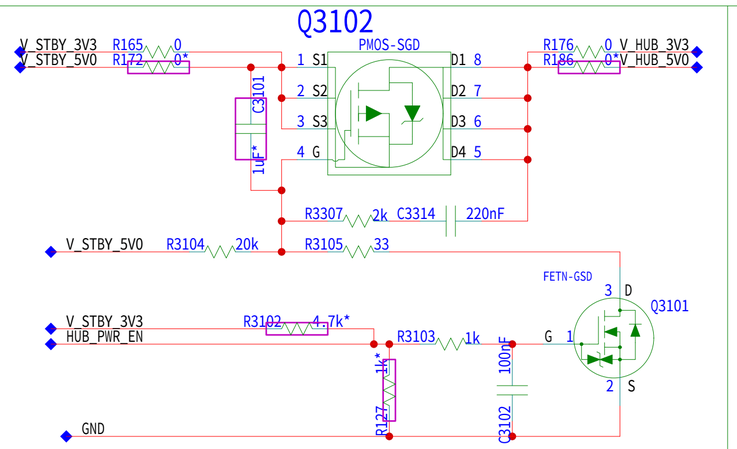
SHEET 29 OF 37

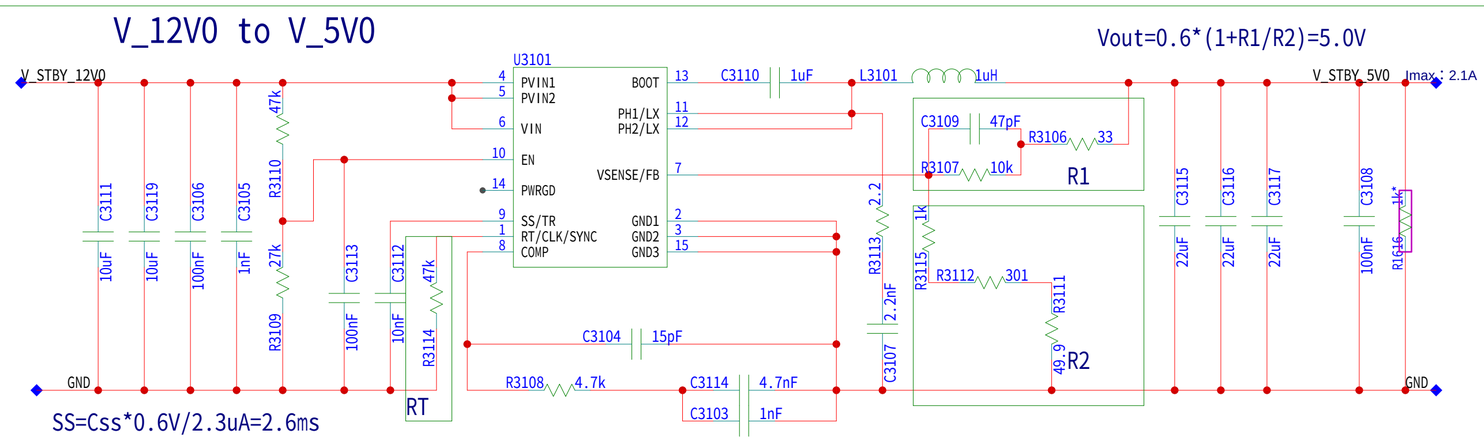
12V Input

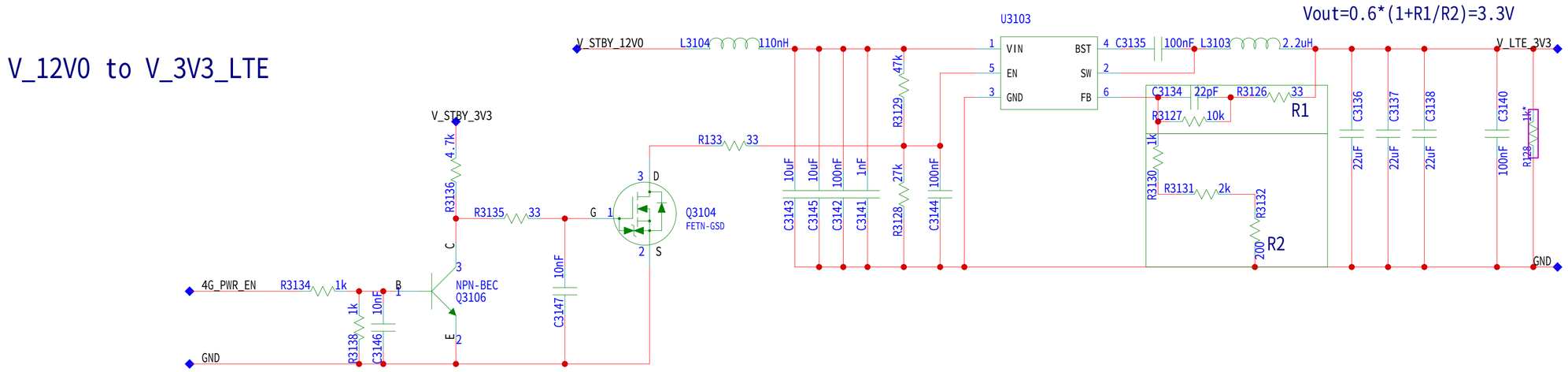

V_12V0_CON_IN
Imax=11.4A
J2
TP26
TP25
TP34
TP29
D3001
F3001
R3004 2.2
R3005 2.2
C3007 1uF
C3008 100nF
C3006 100nF
V_STBY_3V3
R3003 30k
R3023 10k
/PG_24711_POWER
R3022 0
欠压点：9.2V
OPP=76W
C3004 100nF
R3010 4.7k
C3011 1nF*
R3020 15k
R3021 10k
C3009 100nF
C3002 100nF
U3001
PGB
EN
PROG
TIMER
GND
MODE/FLTB
VCC
SENSE
GATE
OUT
OCP=16.67A
R3006 10k
C38 100nF
C3003 6.8nF*
C3010 100nF
C3005 100nF
R3007 0*
C81 100nF
R3008 10k*
V_12V0_SENSE
C3001 100nF*
R132 2.2*
GND
refer to user guide
pin 8/9 are differential pair
single connect to sesen riseter
R3001 10k*
R86 10
GATE_24711
R3002 0
V_12V0_IN
D2 D_A D5
防止过流短路状态下负压超规格
25/RSENSE=(1.2--1.5)*Imax
Imax=11.4A
R3019 3m
R3018 3m

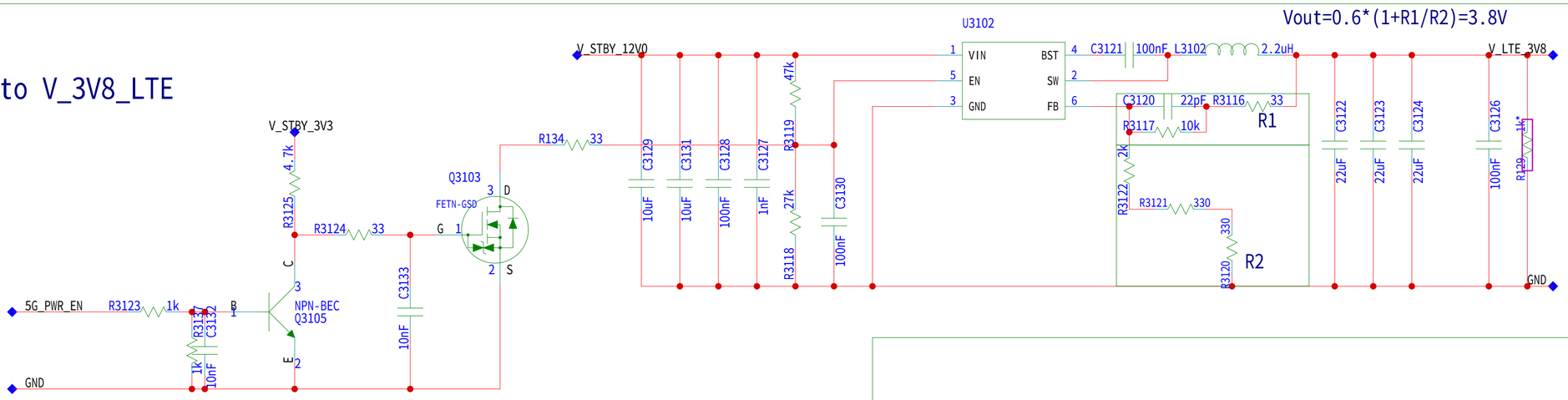

V_12V0_SENSE
D15
D26
D37
D48
Q3001
4G
3S3
2S2
1S1
V_12V0_IN
L3001 1uH
模组12V
VDD
F300212A
底板内12V
V_STBY_12V0
4.9A
12A*[1-0.5%*(90-25)]*75%=6.075A
C3018 1nF
C3017 10uF
C3016 10uF
C3019 10uF
C3020 10uF
C45 1nF
C44 10uF
C43 10uF
C74 10uF
C75 10uF
C125
C126
100nF
GND
10
R3009
GATE_24711


V_12V0_CON_IN
R3012 10
C3014 100nF
R3011 10
V_12V0_SENSE
U3002
GND
GND
R3014 1k
R3015 1k
I2C0_MCU_SDA
I2C0_MCU_SCL
R3016 33
R3017 33
A1
A0
ALERT
SDA
SCL
IN+
IN-
VBUS
GND
VS
R3013 1k
V_12V0_CON_IN
C3015 100nF
GND
GND
V_STBY_3V3
LB3001
C3013 10uF
C3012 100nF
GND
ADDR:1000_000X (0X80)

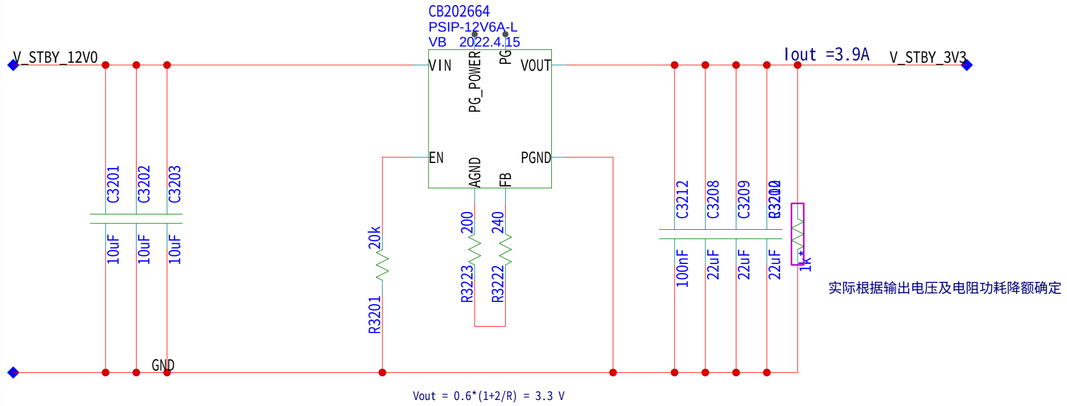

Q3102
PMOS-SGD
V_STBY_3V3
V_STBY_5V0
R165 0
R172 0*
R176 0
R186 0*
V_HUB_3V3
V_HUB_5V0
C3101 1uF*
R3307 2k
C3314 220nF
R3104 20k
R3105 33
FETN-GSD
Q3101
R3102 4.7k*
R3103 1k
R127 1k*
C3102 100nF
HUB_PWR_EN
GND


V_12V0 to V_5V0
Vout=0.6*(1+R1/R2)=5.0V
U3101
V_STBY_12V0
PVIN1
PVIN2
VIN
EN
PWRGD
SS/TR
RT/CLK/SYNC
COMP
BOOT
PH1/LX
PH2/LX
VSENSE/FB
GND1
GND2
GND3
C3110 1uF
L3101 1uH
V_STBY_5V0 Imax : 2.1A
C3111 10uF
C3119 10uF
C3106 100nF
C3105 1nF
R3110 47k
R3109 27k
C3113 100nF
C3112 10nF
R3114 47k
RT
C3104 15pF
R3108 4.7k
C3114 4.7nF
C3103 1nF
R3113 2.2
C3107 2.2nF
C3109 47pF
R3106 33
R3107 10k
R1
R3115 1k
R3112 301
R3111
49.9
R2
C3115 22uF
C3116 22uF
C3117 22uF
C3108 100nF
R116 1k*
SS=Css*0.6V/2.3uA=2.6ms

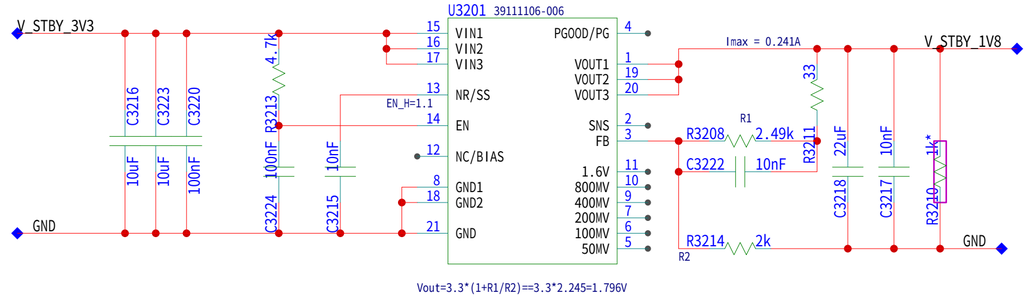

V_12V0 to V_3V3_LTE
Vout=0.6*(1+R1/R2)=3.3V
U3103
V_STBY_12V0
L3104 110nH
VIN
EN
GND
BST
SW
FB
C3135 100nF
L3103 2.2uH
V_LTE_3V3
C3134 22pF
R3126 33
R3127 10k
R1
R3130 1k
R3131 2k
R3132 200
R2
C3136 22uF
C3137 22uF
C3138 22uF
C3140 100nF
R128 1k*
GND
V_STBY_3V3
R133 33
C3143 10uF
C3145 10uF
C3142 100nF
C3141 1nF
R3129 47k
R3128 27k
C3144 100nF
R3136 4.7k
R3135 33
Q3104
FETN-GSD
C3147 10nF
4G_PWR_EN
R3134 1k
NPN-BEC
Q3106
R3138 1k
C3146 10nF


V_12V0 to V_3V8_LTE
Vout=0.6*(1+R1/R2)=3.8V
U3102
V_STBY_12V0
VIN
EN
GND
BST
SW
FB
C3121 100nF
L3102 2.2uH
V_LTE_3V8
C3120 22pF
R3116 33
R3117 10k
R1
R3122 2k
R3121 330
330
R3120
R2
C3122 22uF
C3123 22uF
C3124 22uF
C3126 100nF
R129 1k*
GND
V_STBY_3V3
R134 33
C3129 10uF
C3131 10uF
C3128 100nF
C3127 1nF
R3119 47k
R3118 27k
C3130 100nF
R3125 4.7k
R3124 33
Q3103
FETN-GSD
C3133 10nF
5G_PWR_EN
R3123 1k
NPN-BEC
Q3105
R3137 1k
C3132 10nF

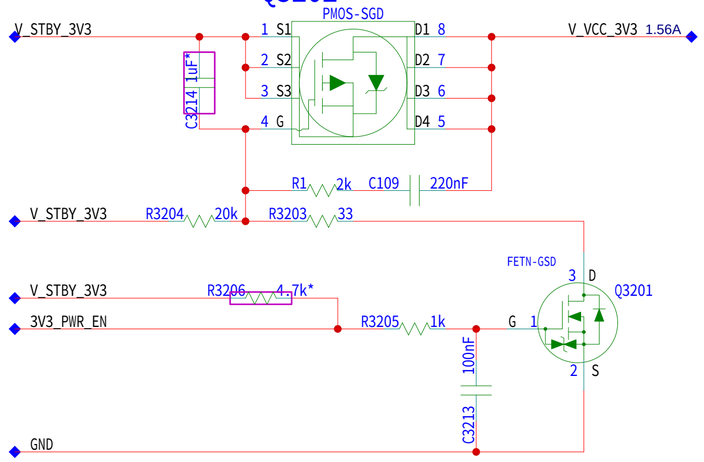
Power 12V to 3V3



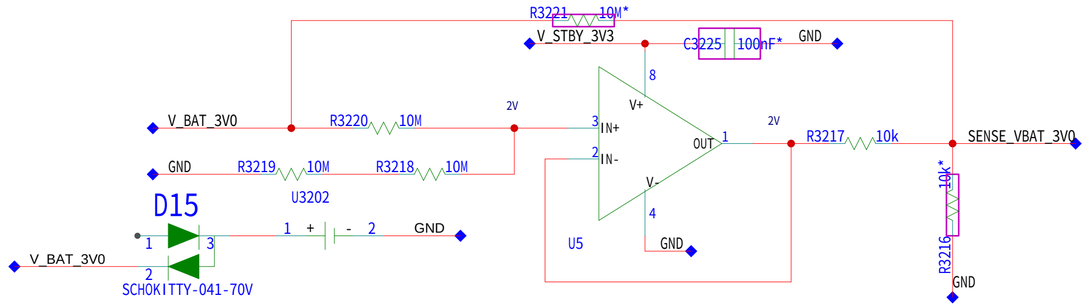
Power 3V3 to 1V8



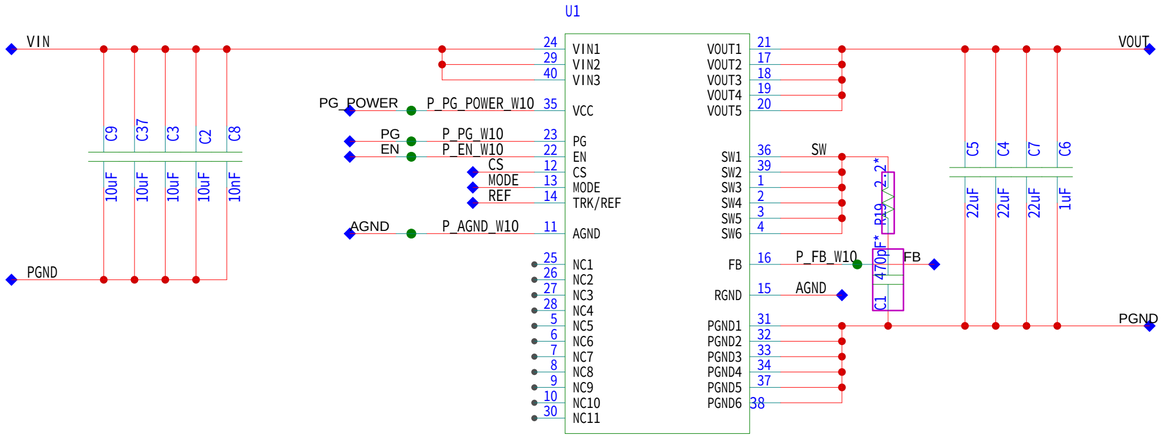
Q3202

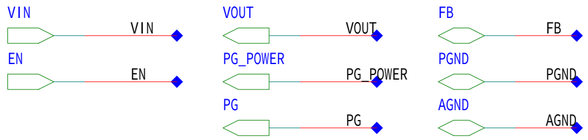


RTC电源及电压检测



DC-DC CBB





NOTE:详细资料参考应用设计指导书

1、Vin：Cin最小值为20uF+10nF瓷片电容；

2、EN下拉电阻外置；在5V输出及以上场景时，CBB中EN下拉电阻R2001=17.4k（注：如要使用在5V输出以下场景，则需取R2001=20k）；该管脚不要外加电容

3、VCC:默认悬空，使用PG时必须上拉到该管脚（3V）

4、FB:输出调节，通过FB和RGND之间的电阻来调节输出电压，TRIM调节电阻R1和R2必须选择1%精度电阻。

5、PG:不使用PG时悬空，使用时上拉大于等于3K电阻至VCC（3V），且串联一个1K电阻至I/O口，不推荐外部电源（小于3.6V）上拉，外部上拉在EN使能前会有一个0.6V电平；

6、MODE:默认悬空，频率设定管脚

7、CS:默认悬空，OCP点设定管脚，过流点电阻Rcs（59K）已内置

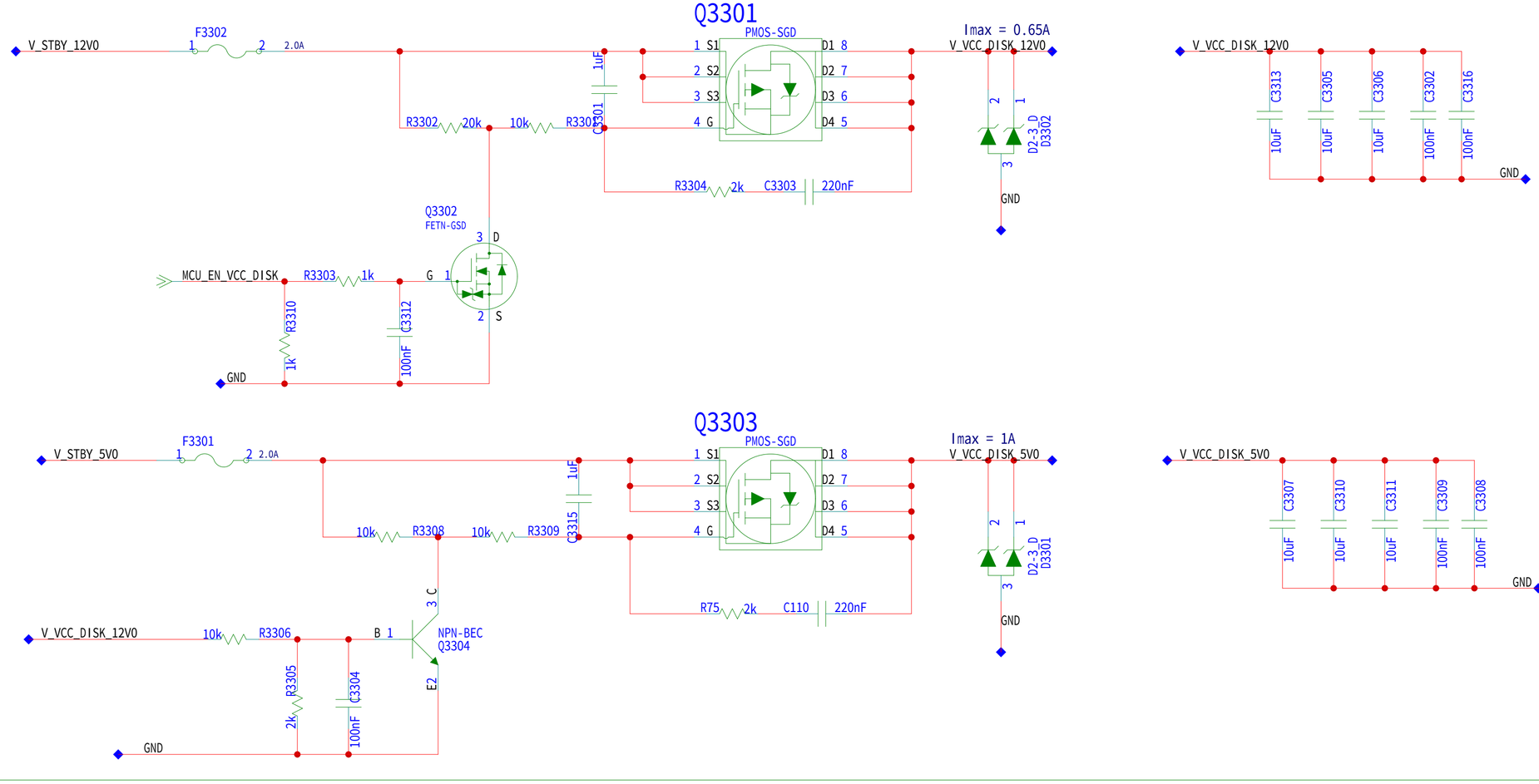
8、Vout：Cout最小值为44uF瓷片电容；

9、输出电压与输出电容配置见下表：输出电容选型，请与单板电源工程师讨论

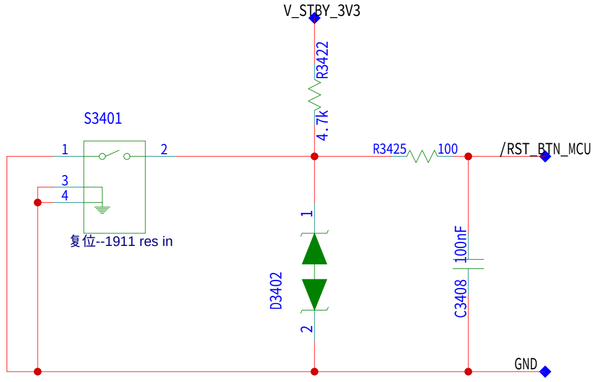
输出电压	0.7V	1.2V	1.8V	3.3V	5.4V
输出电源	9*22UF	7*22UF	5*22UF	4*22UF	3*22UF

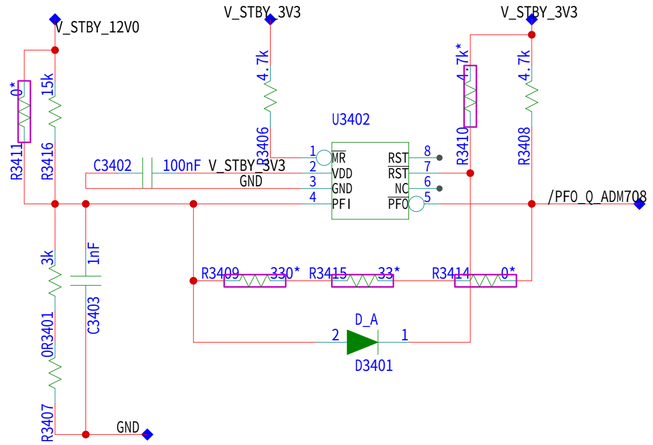
SHEET 1 OF 1

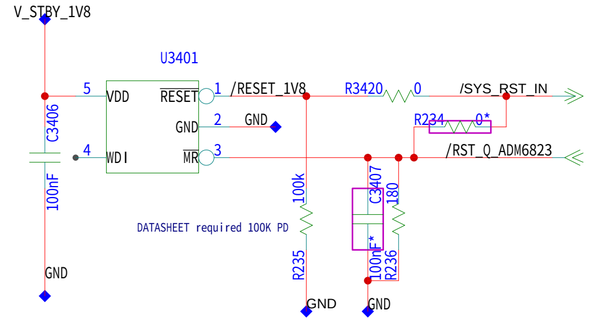
SATA Power

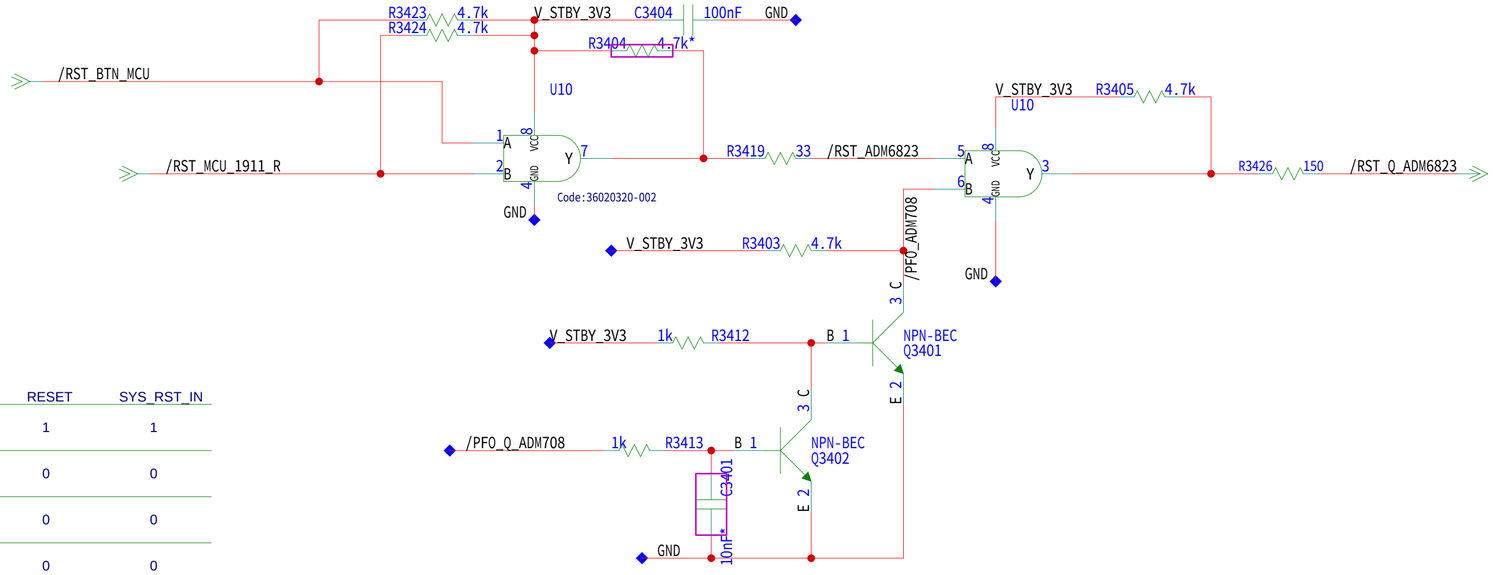

Q3301
PMOS-SGD
F3302
V_STBY_12V0
2.0A
1 S1
2 S2
3 S3
4 G
D1 8
D2 7
D3 6
D4 5
Imax = 0.65A
V_VCC_DISK_12V0
R3302 20k
10k R3301
C3301 1uF
R3304 2k
C3303 220nF
D2-3_D
D3302
GND
Q3302
FETN-GSD
MCU_EN_VCC_DISK
R3303 1k
R3310 1k
C3312 100nF
Q3303
PMOS-SGD
F3301
V_STBY_5V0
2.0A
Imax = 1A
V_VCC_DISK_5V0
10k R3308
10k R3309
C3315 1uF
R75 2k
C110 220nF
D3301
V_VCC_DISK_12V0
10k R3306
R3305 2k
C3304 100nF
NPN-BEC
Q3304
C3313 10uF
C3305 10uF
C3306 10uF
C3302 100nF
C3316 100nF
C3307 10uF
C3310 10uF
C3311 10uF
C3309 100nF
C3308 100nF

RST BTN



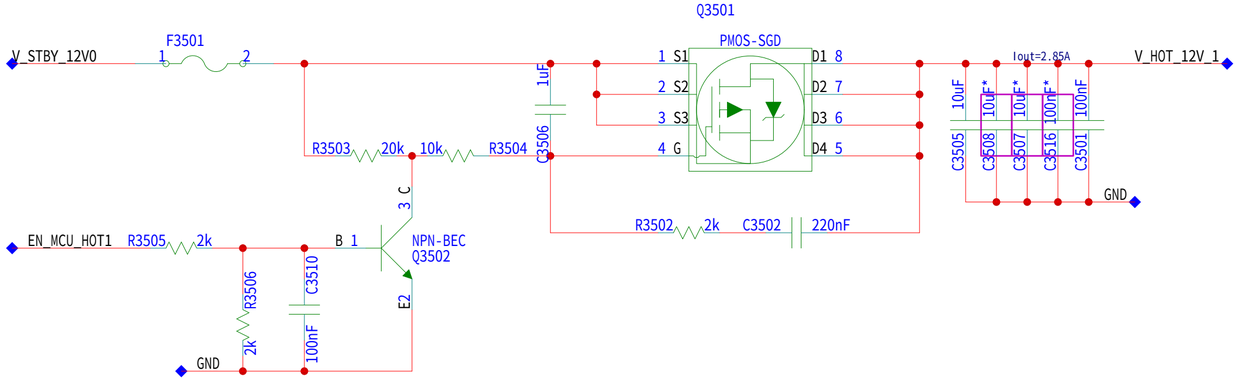


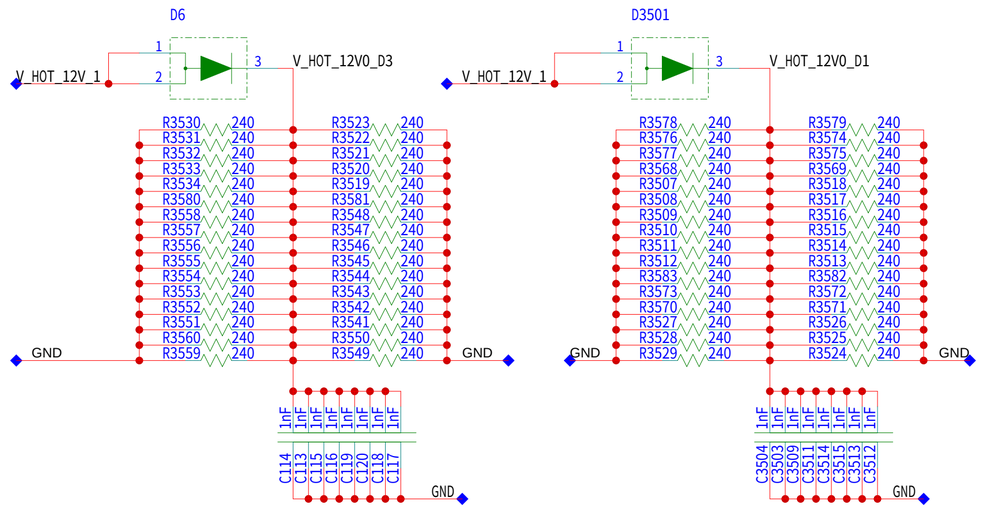


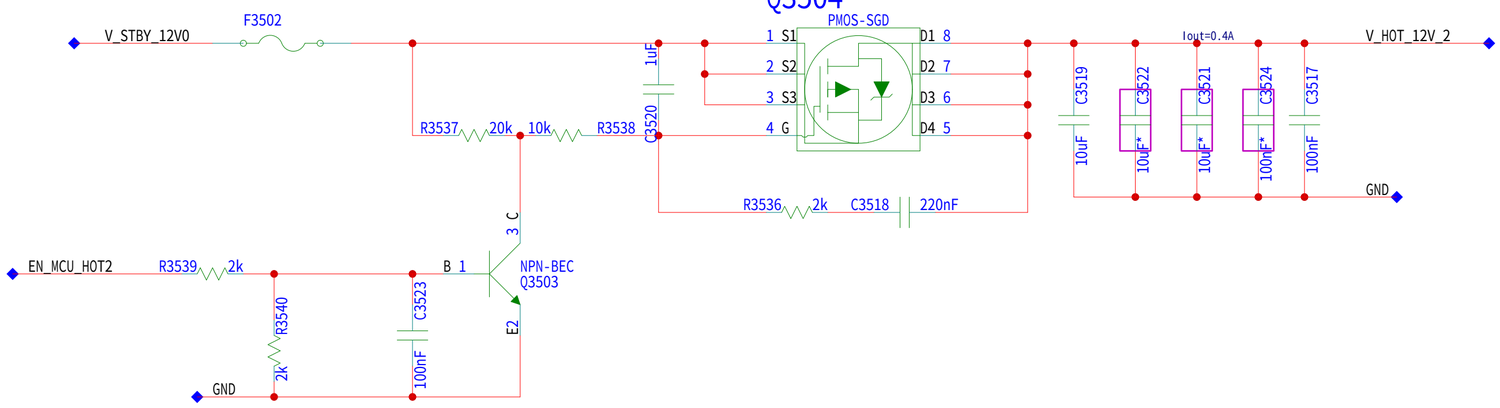


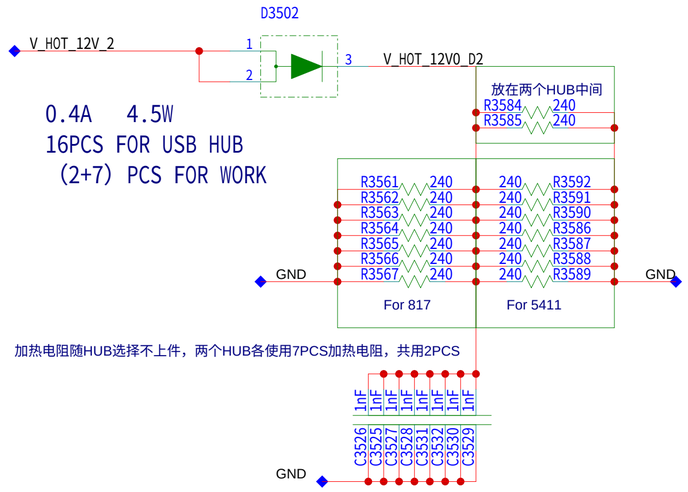
	BTN	MCU	PFO	RESET	SYS_RST_IN
Def	1	1	1	1	1
BTN	0	1	1	0	0
MCU	1	0	1	0	0
PFO	1	1	0	0	0

Heating Resistor

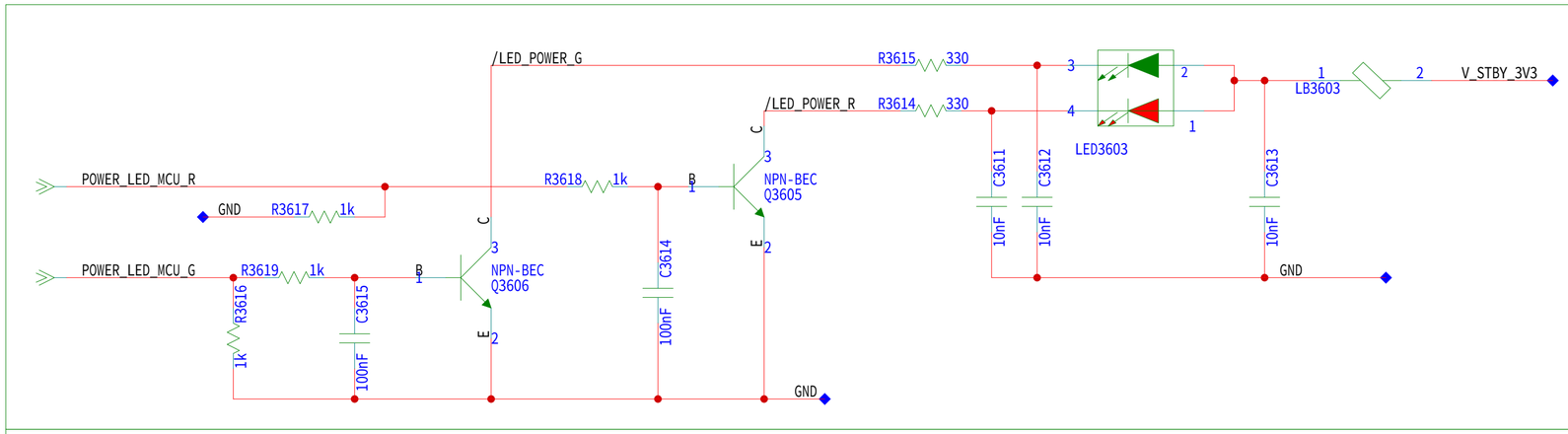


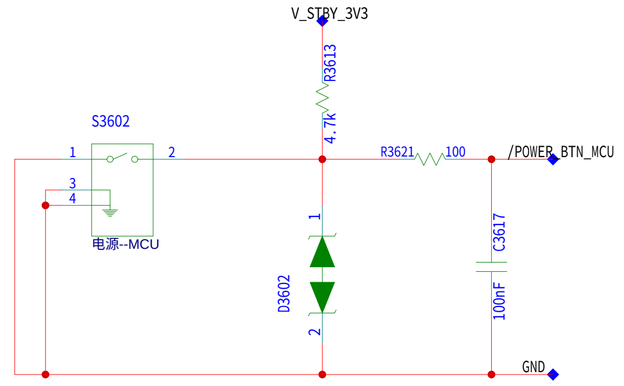


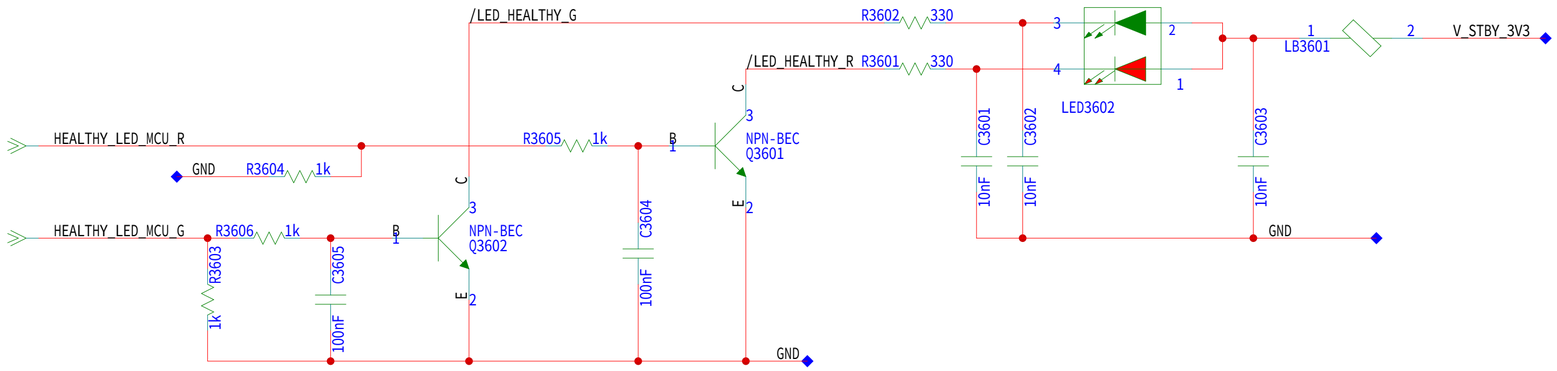


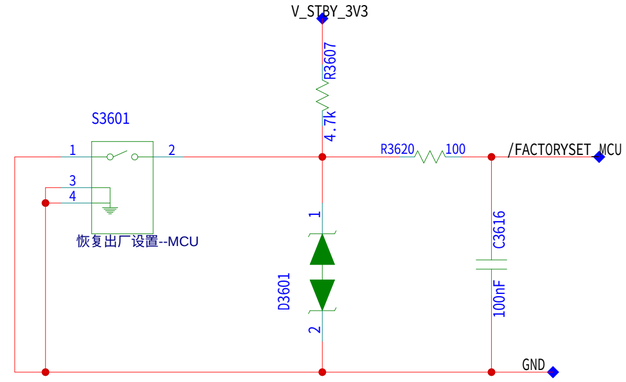


LED & Tact Switch

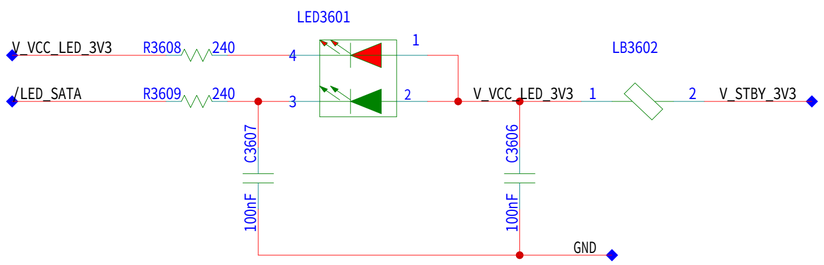


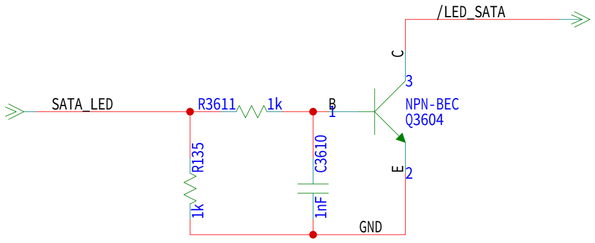




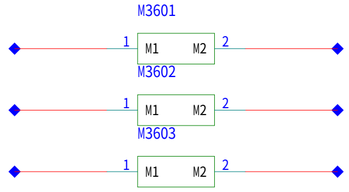


Red LED not use.

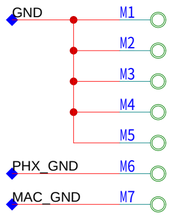




LED导光柱

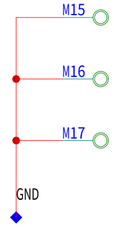


FOR BOARD

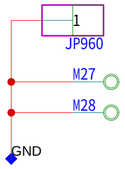


FOR GUIDE PIN

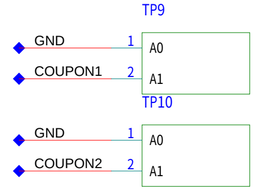
FOR 4G



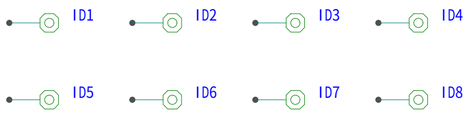
FOR 5G



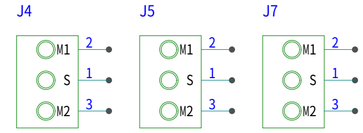
TEST POINT



PCB MARK POINT



FOR MINI BOARD



FOR TPM

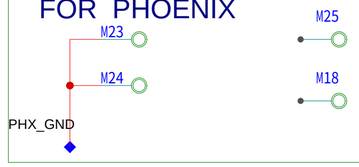
ICT

FOR M.2 SSD

FOR LTE WIRE

FOR MXM

FOR PHOENIX



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