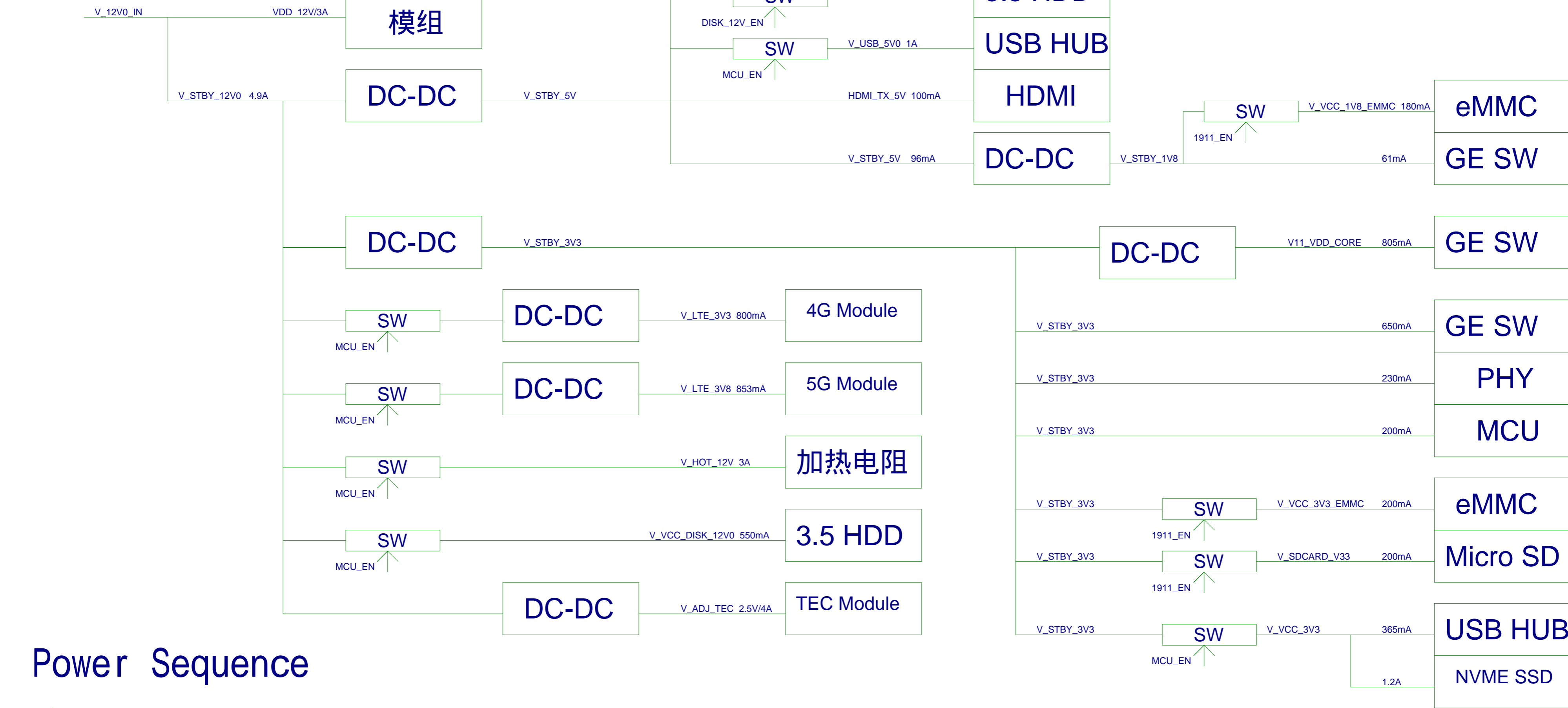


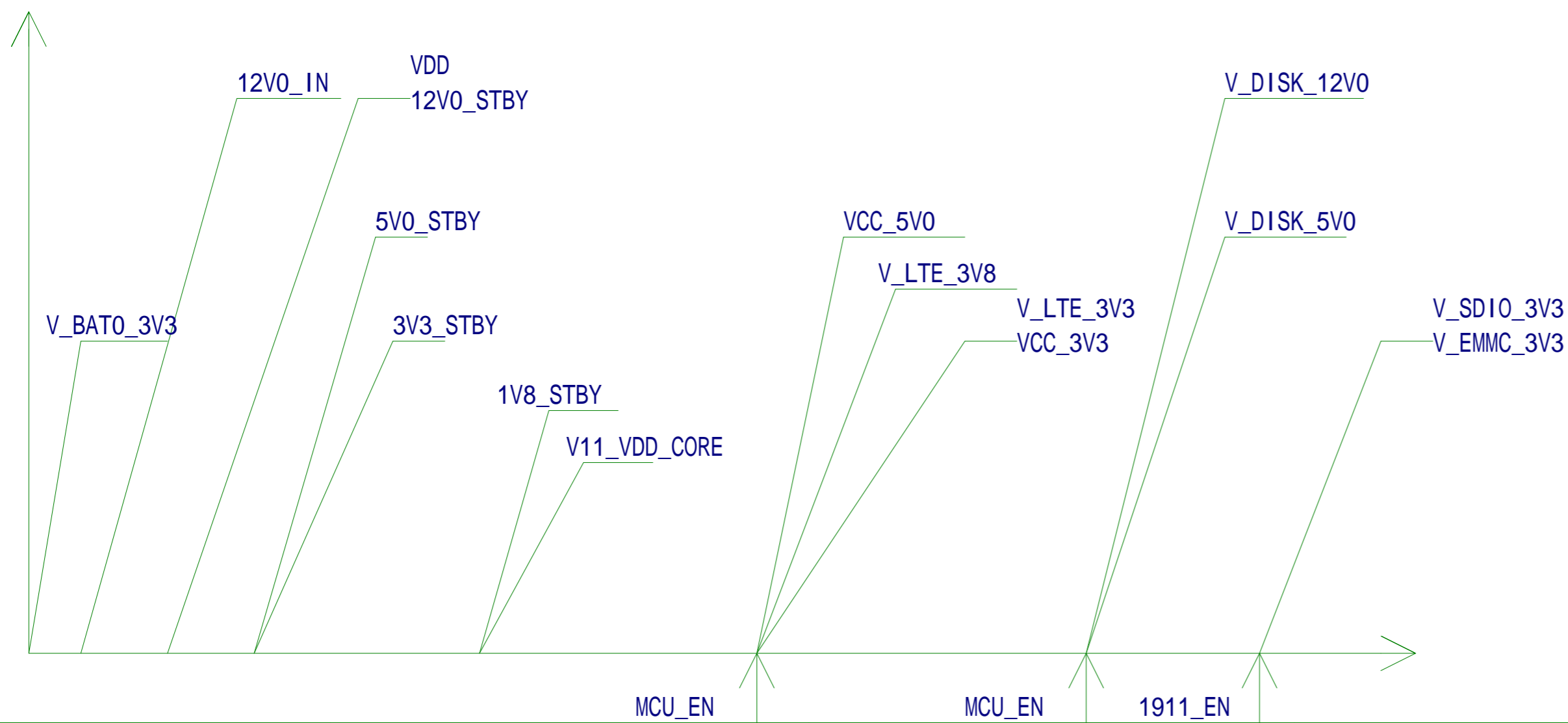
Atlas 200I A2 底板电路参考设计

Department : Ascend Computing Hardware Program

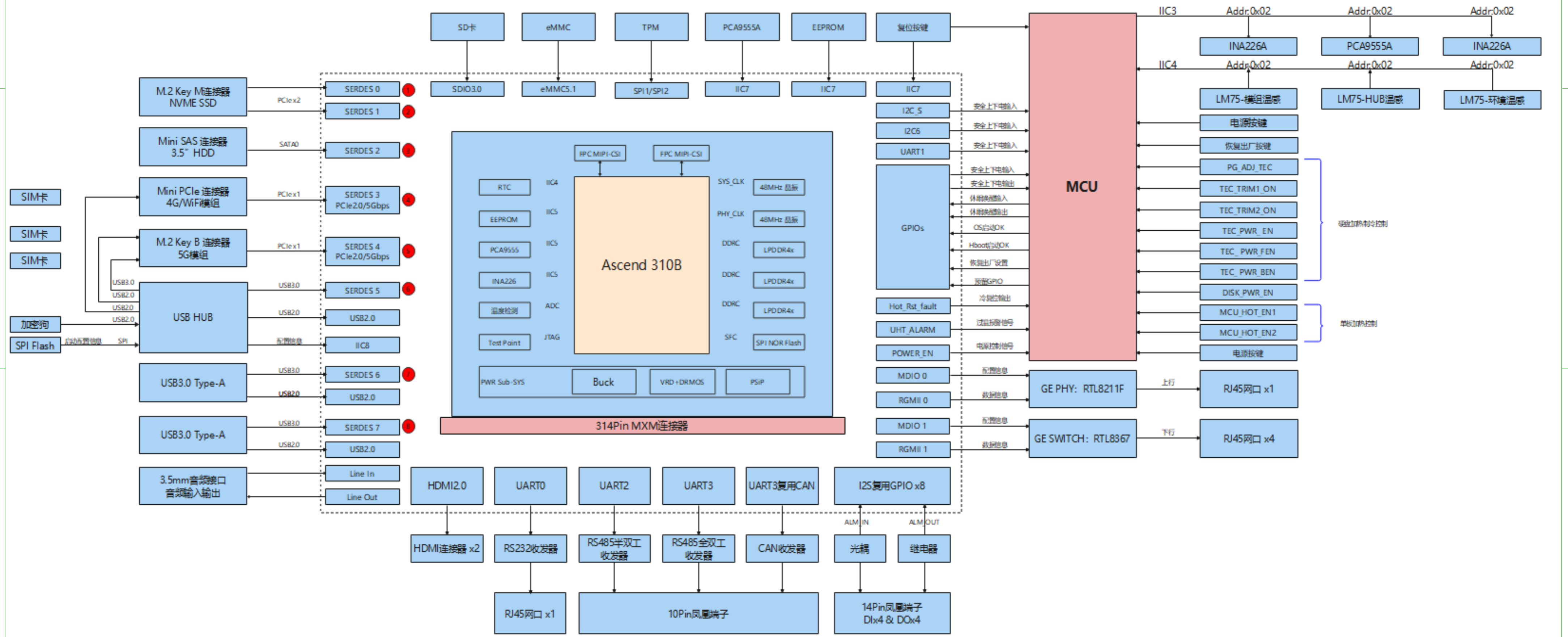
Power Tree



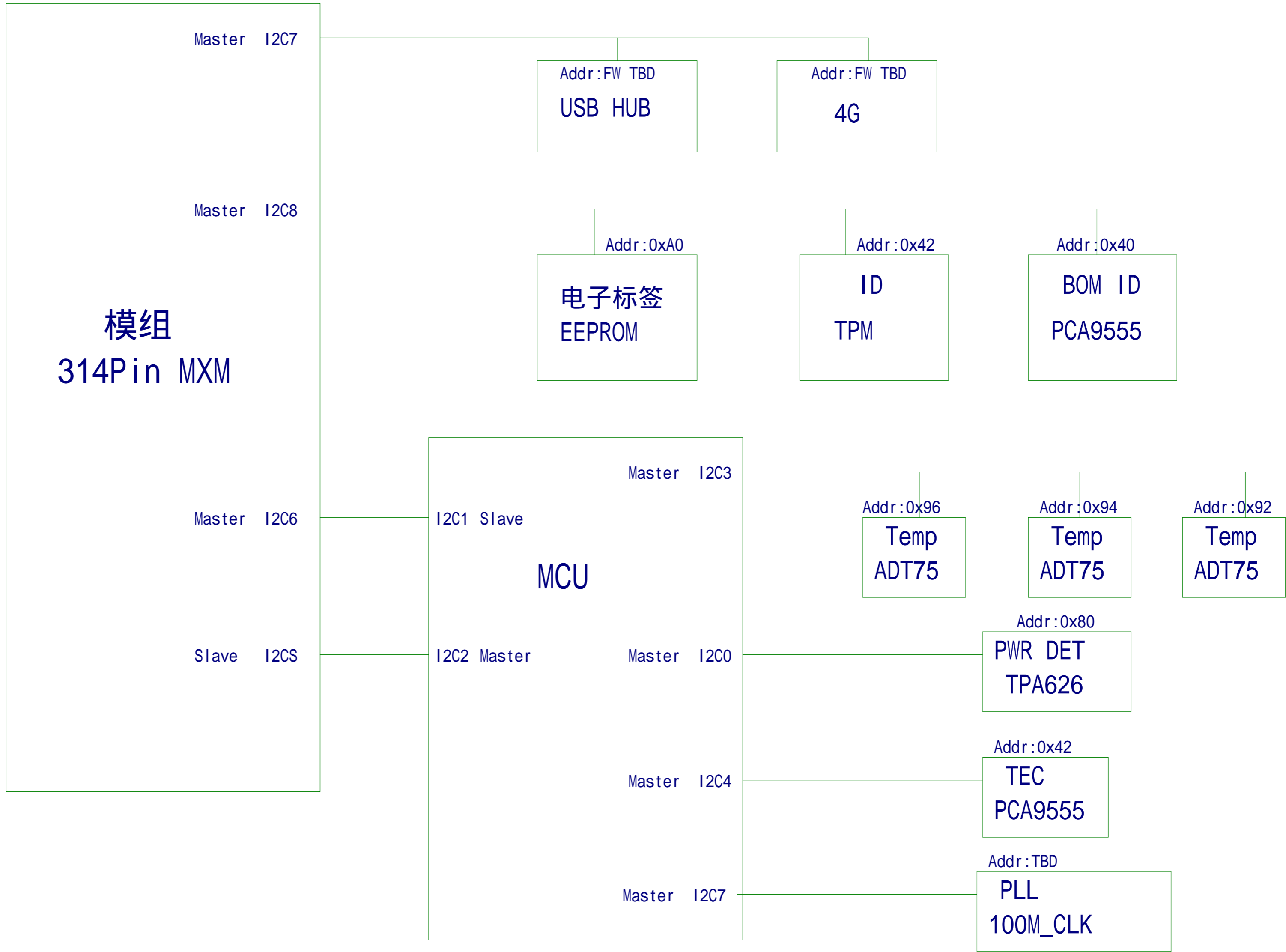
Power Sequence



Block Diagram



I2C Block Diagram



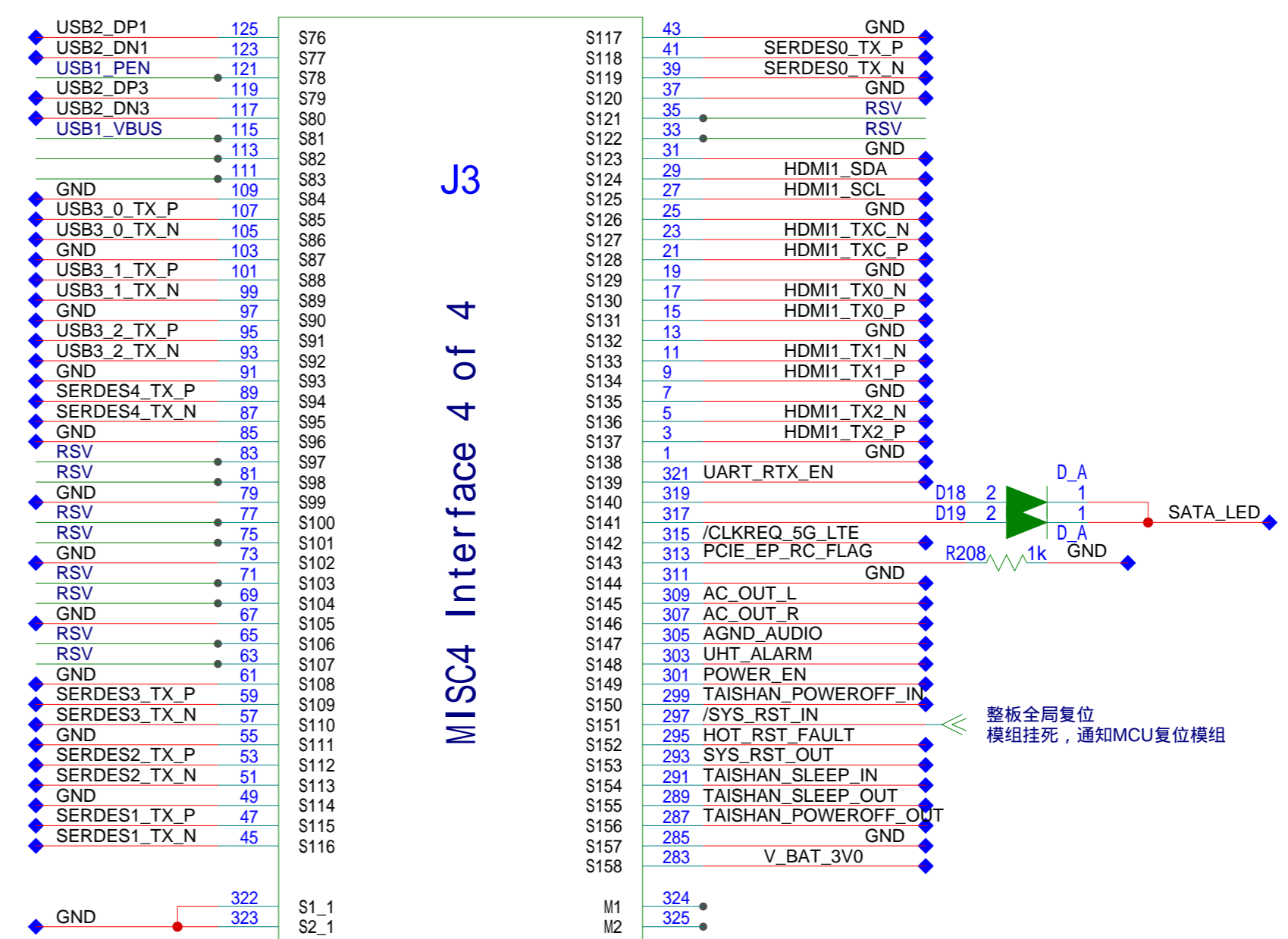
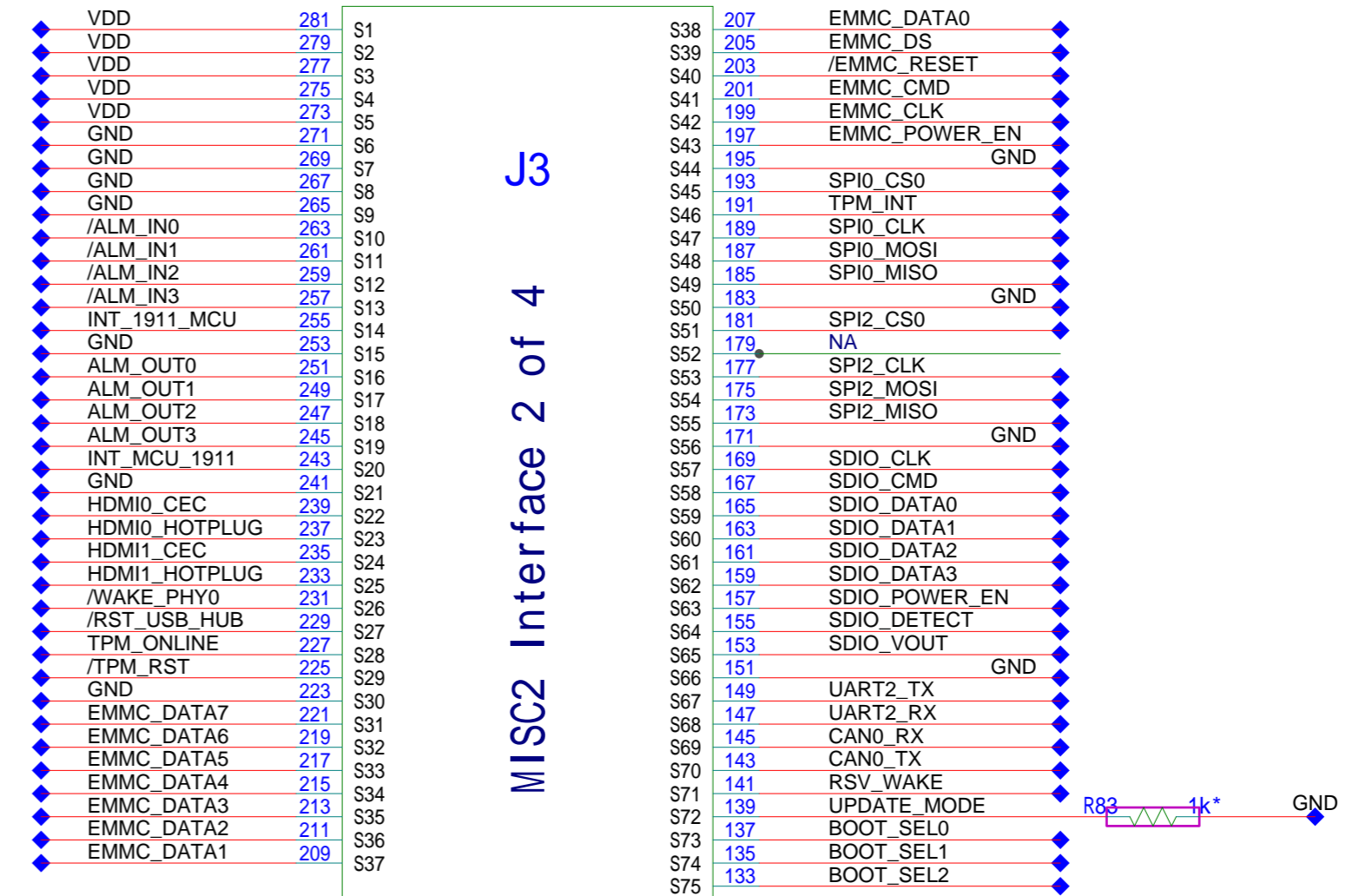
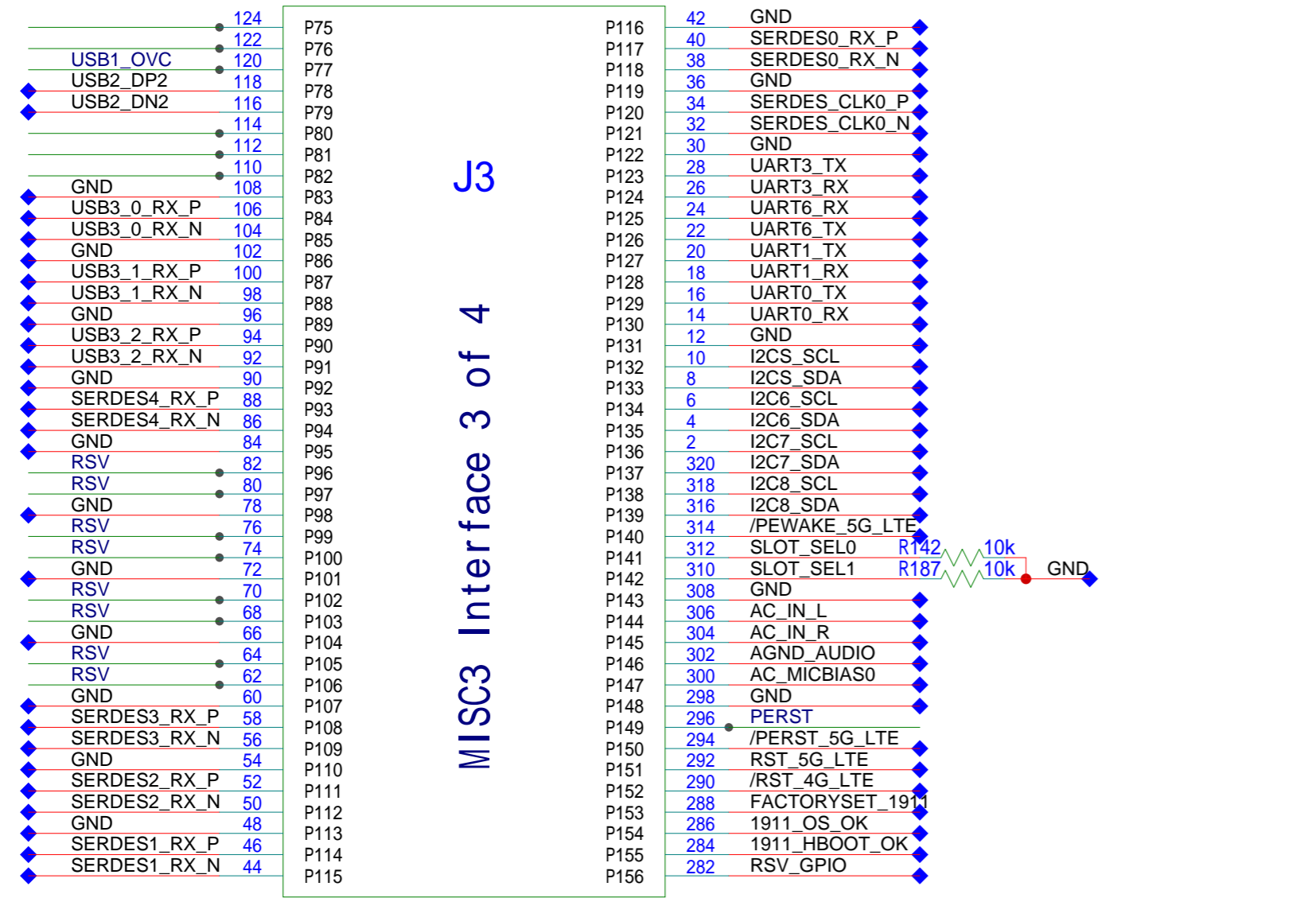
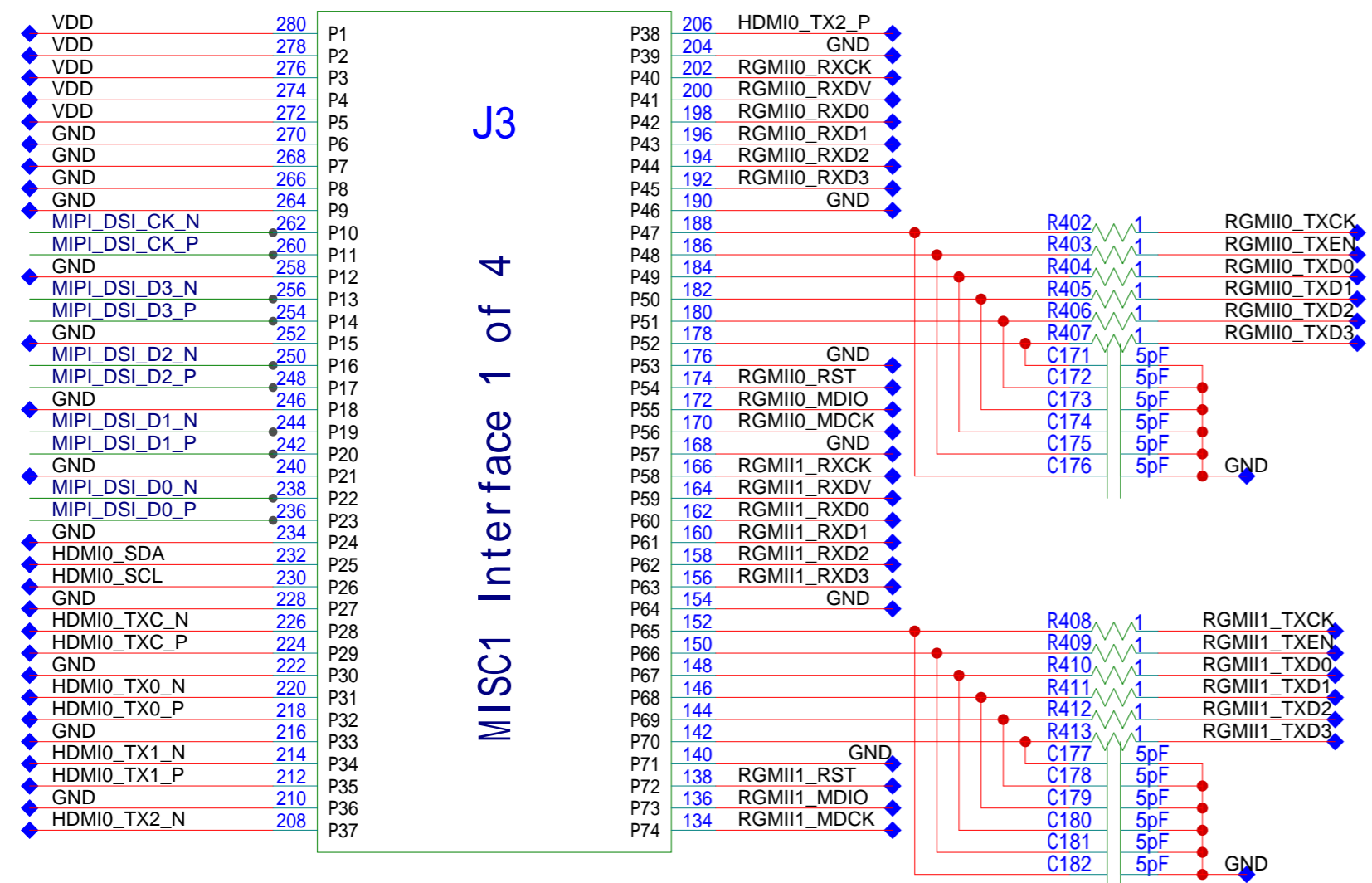
模组
314Pin MXM

A

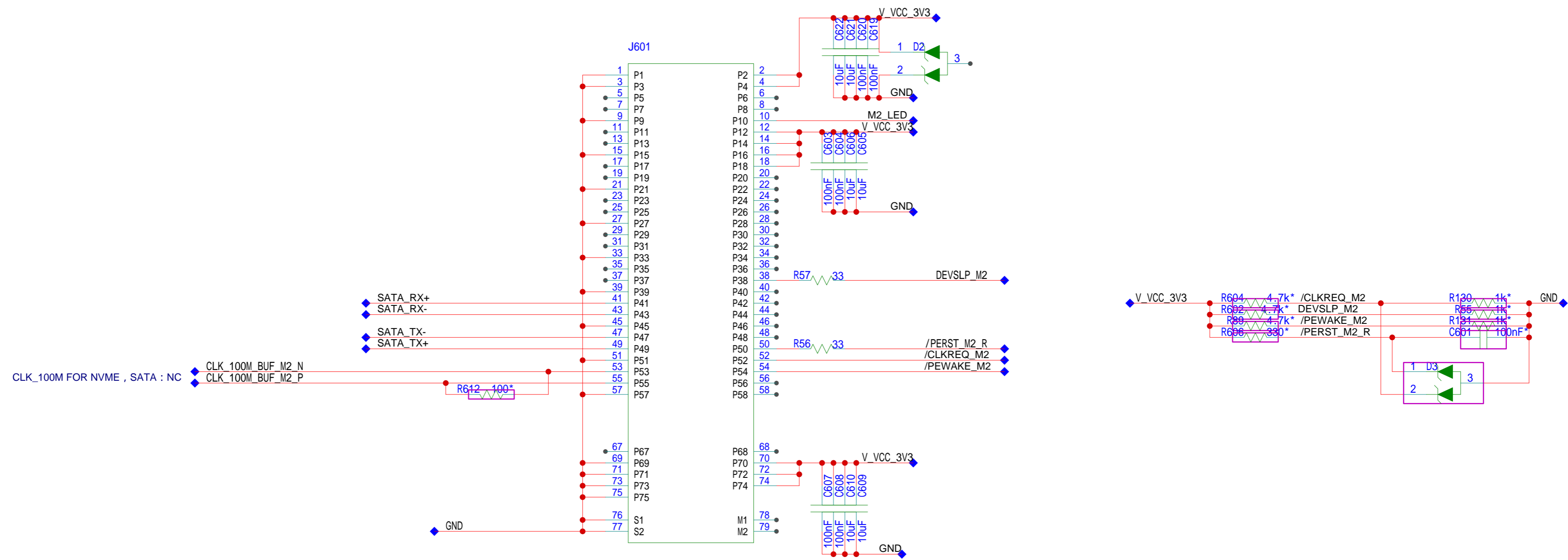
B

A

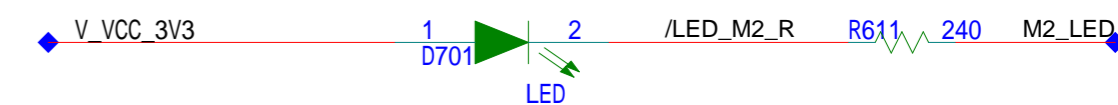
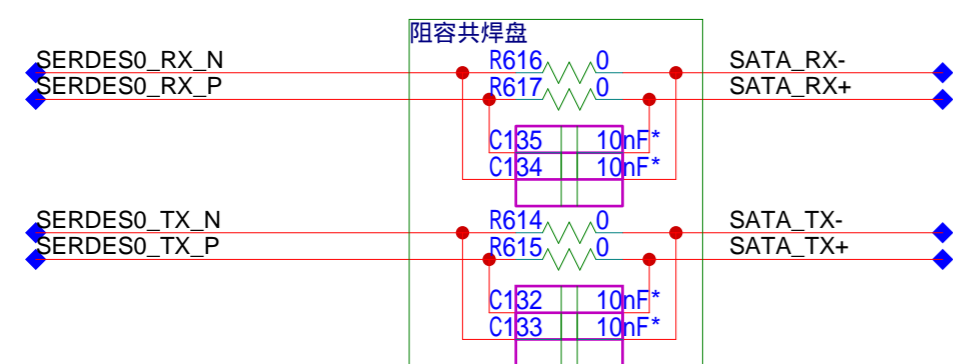
B



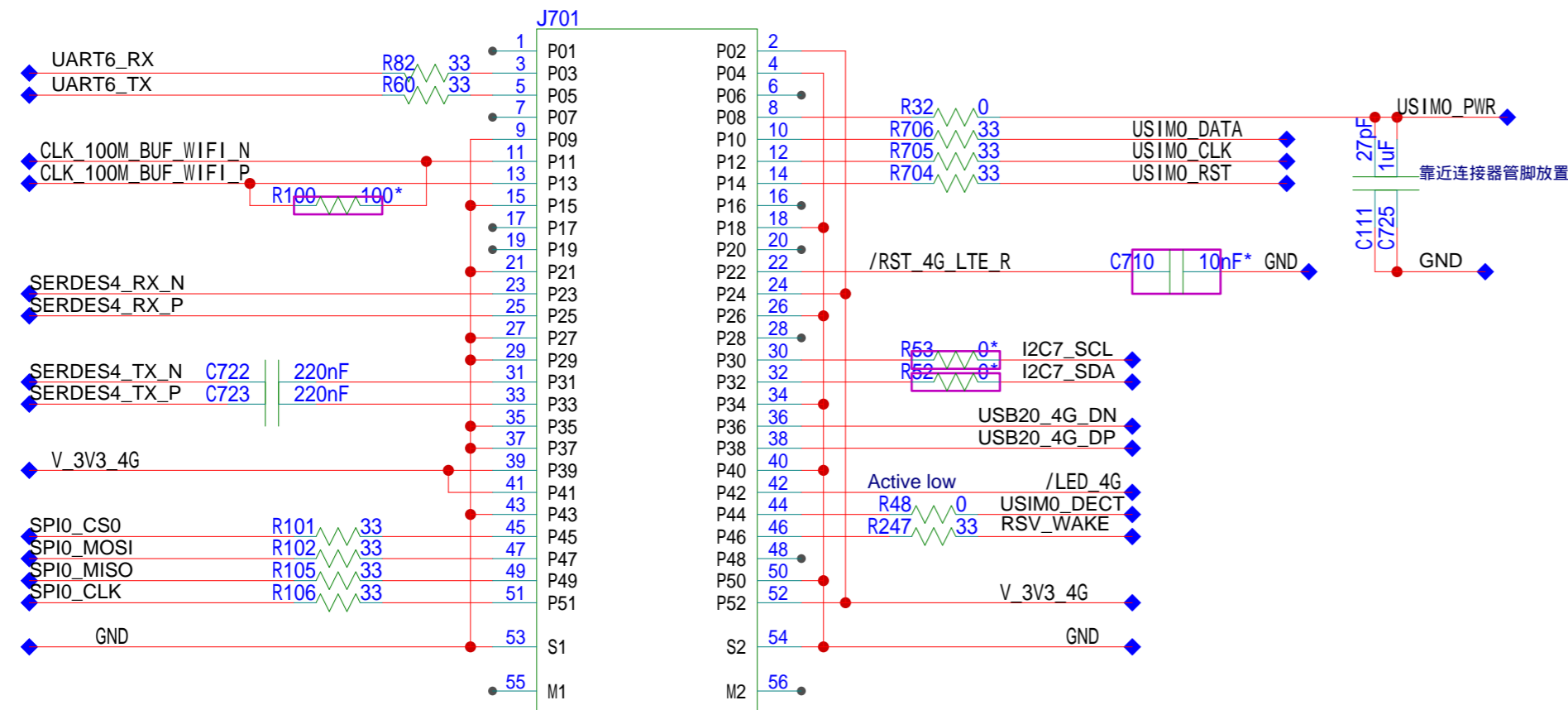
M.2 SATA SSD



兼容不同厂家SATA盘设计方案，
硬盘端串有10nF电容时上件0ohm电阻，
硬盘端无10nF电容时在底板上件10nF电容。



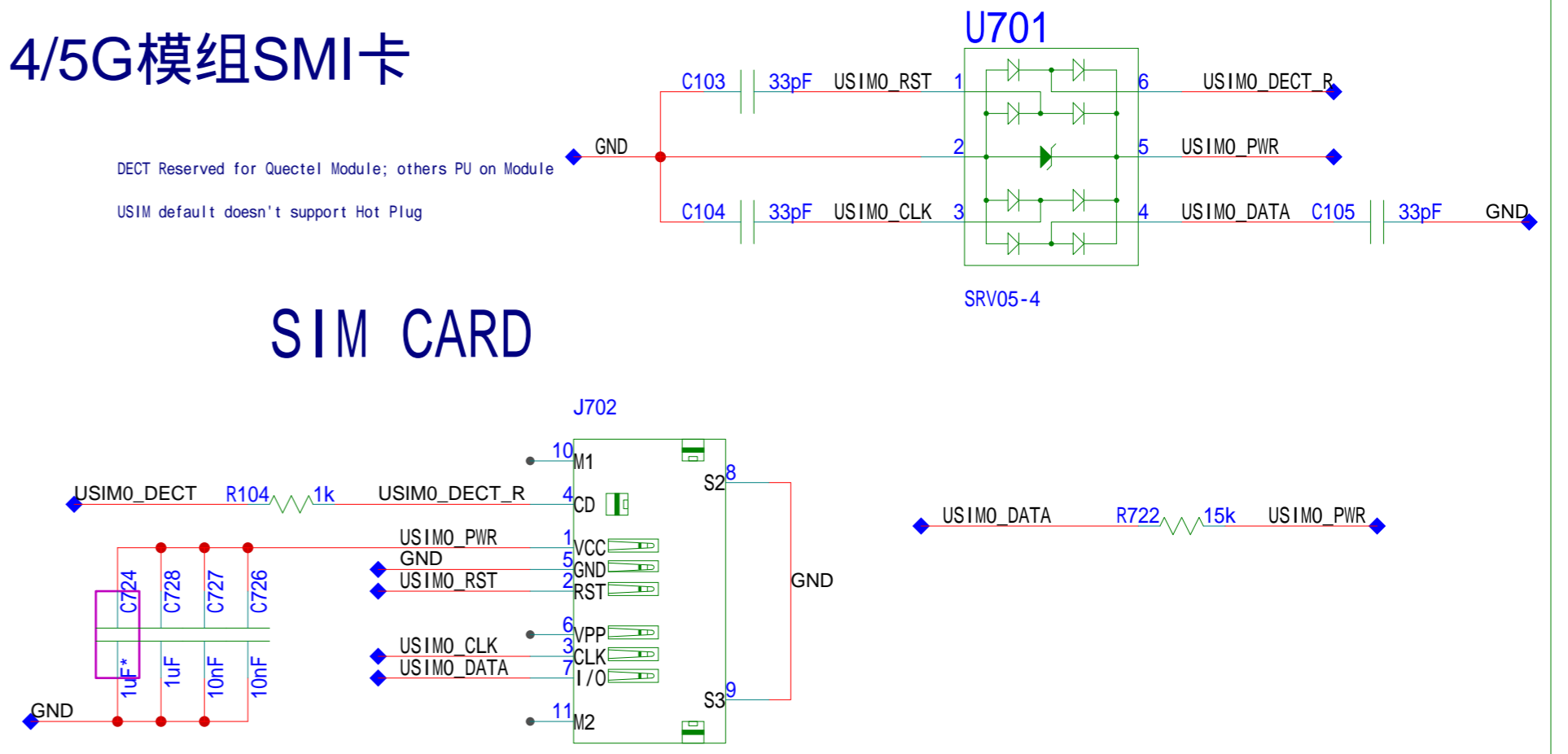
Mini WiFi/4G



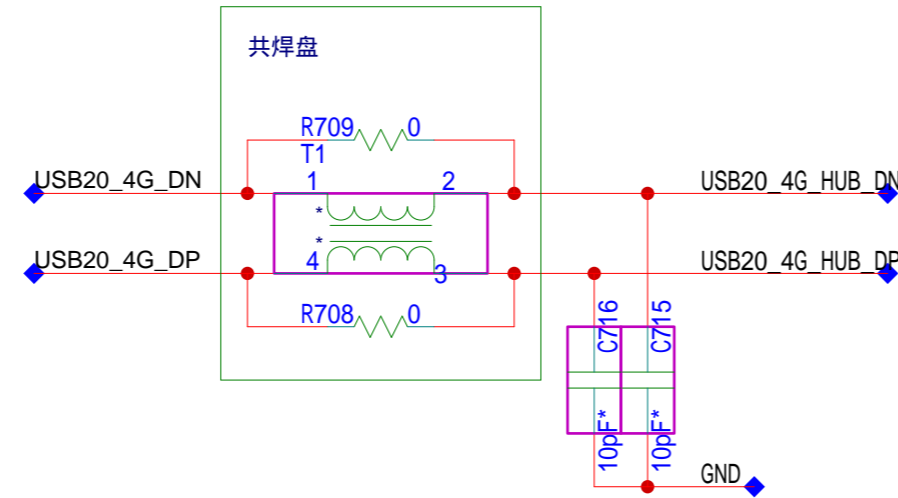
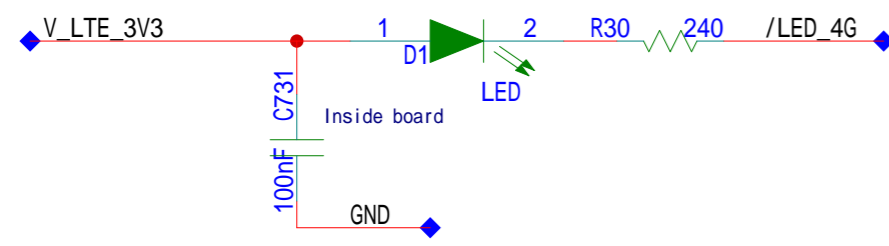
4/5G模组SMT卡

DECT Reserved for Quectel Module; others PU on Module
 USIM default doesn't support Hot Plug

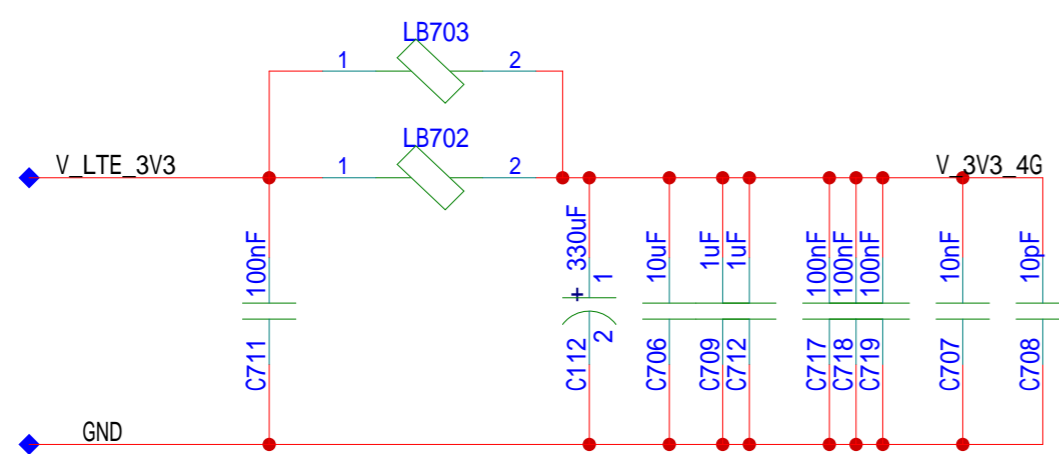
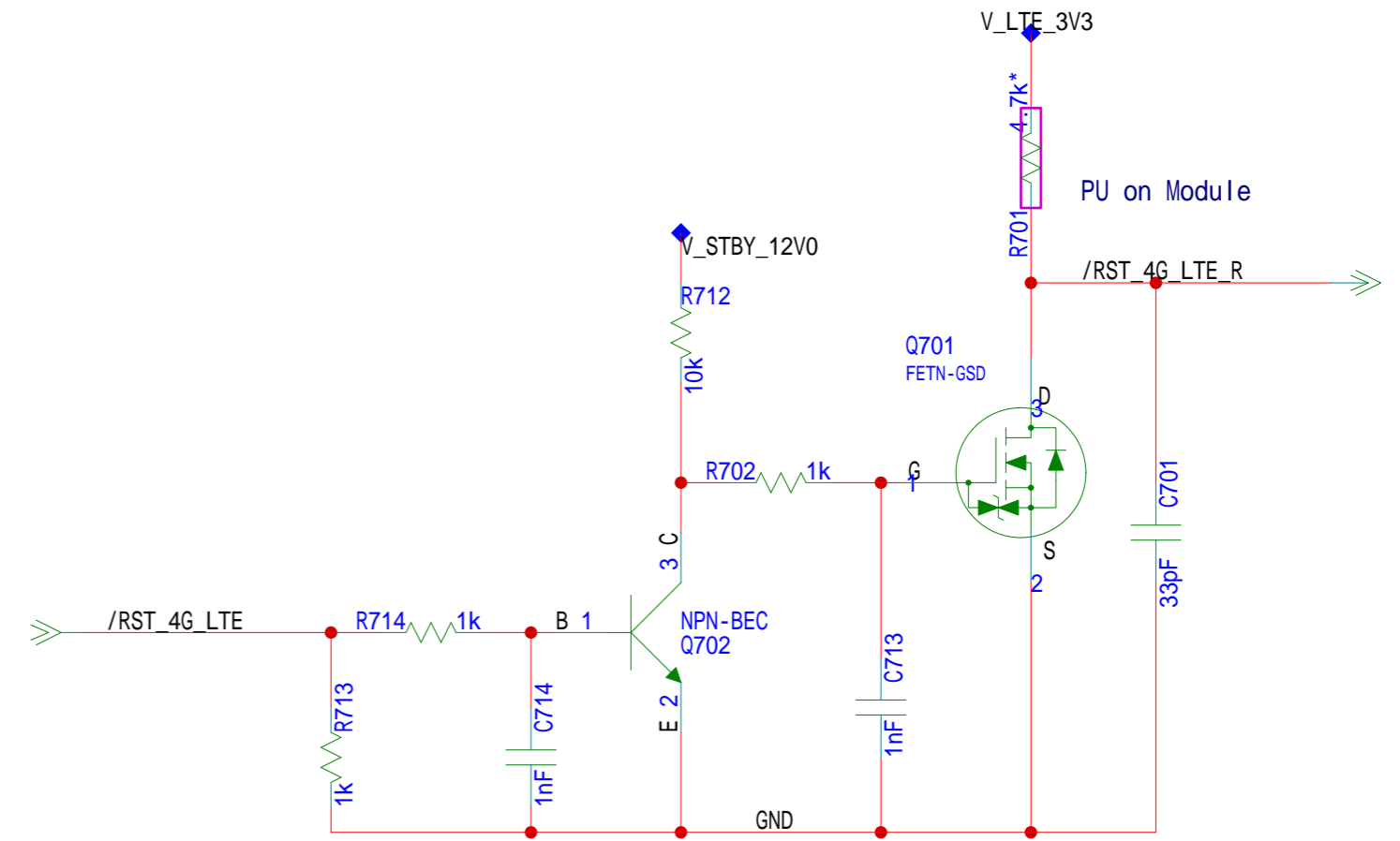
SIM CARD



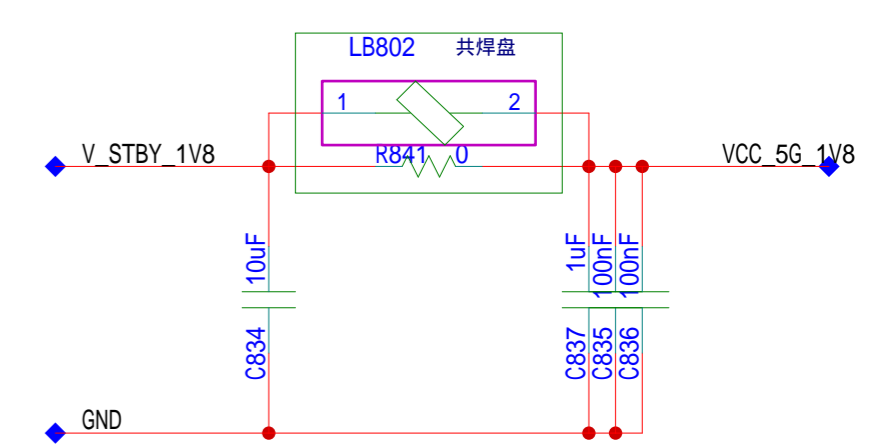
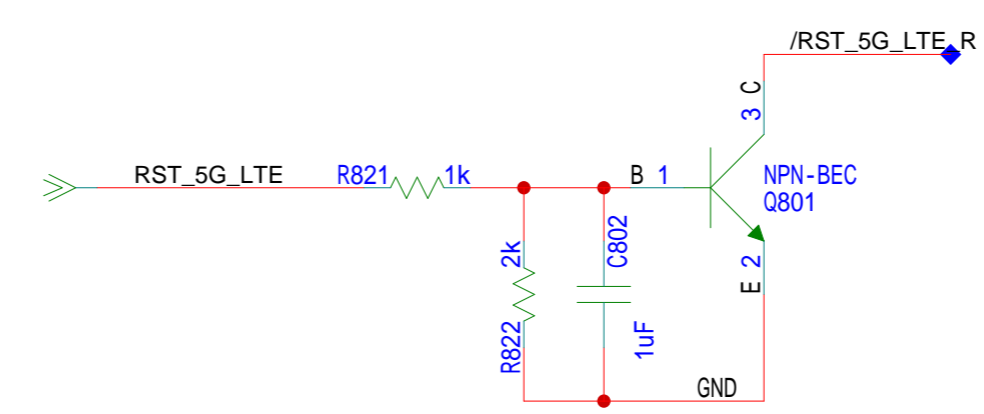
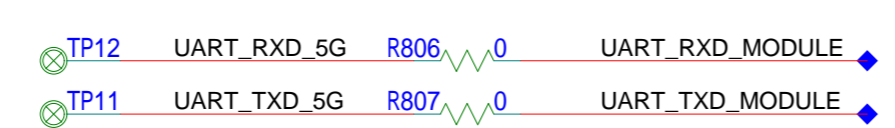
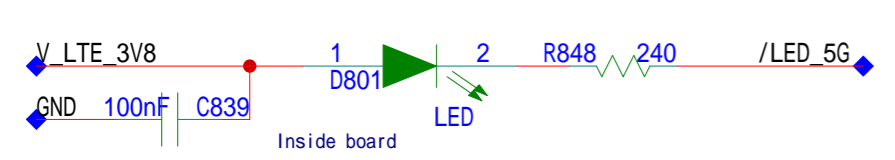
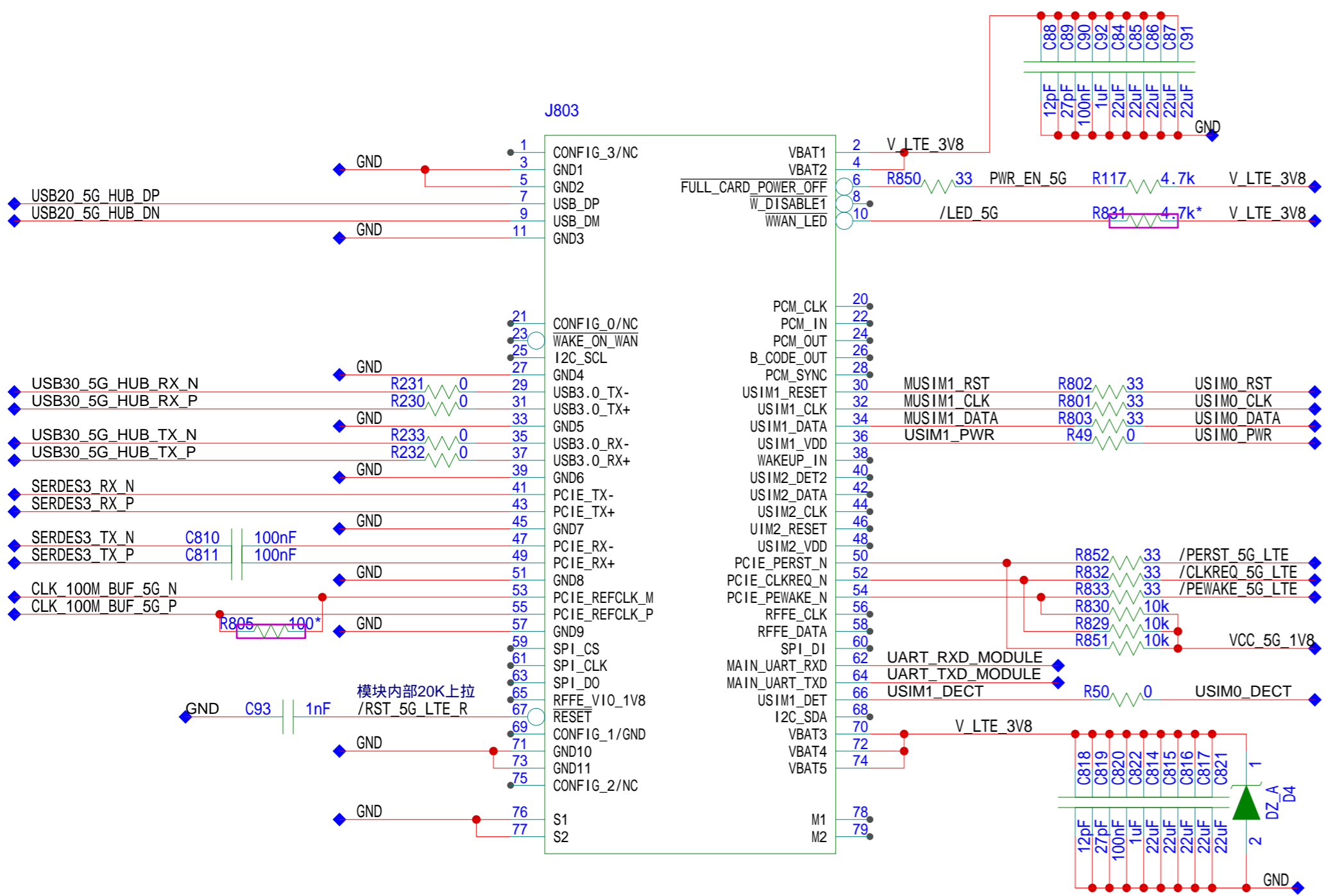
模块状态指示灯

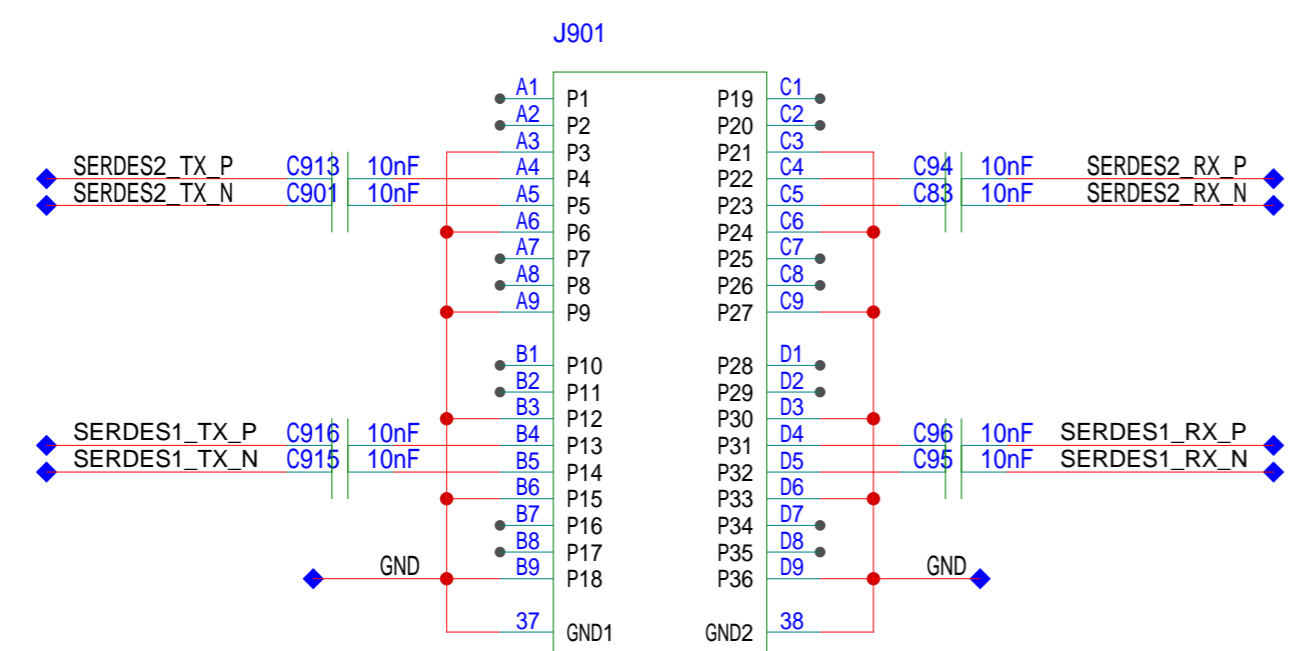


RST

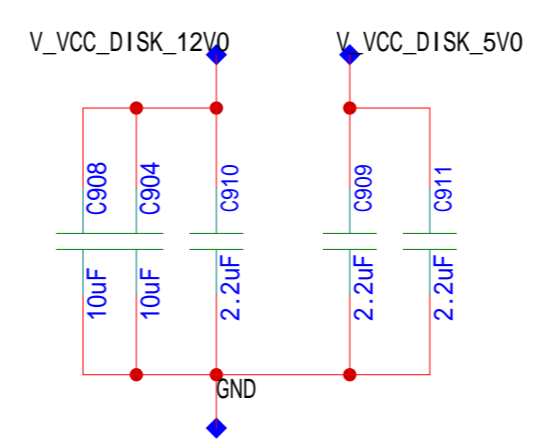
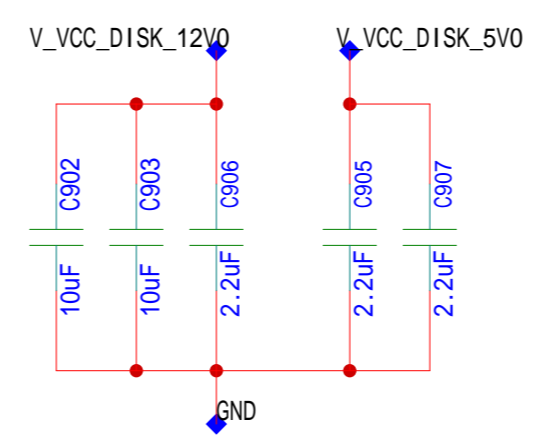


M.2-5G Module

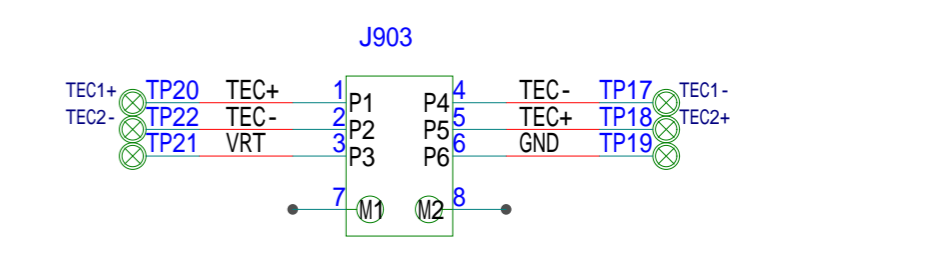
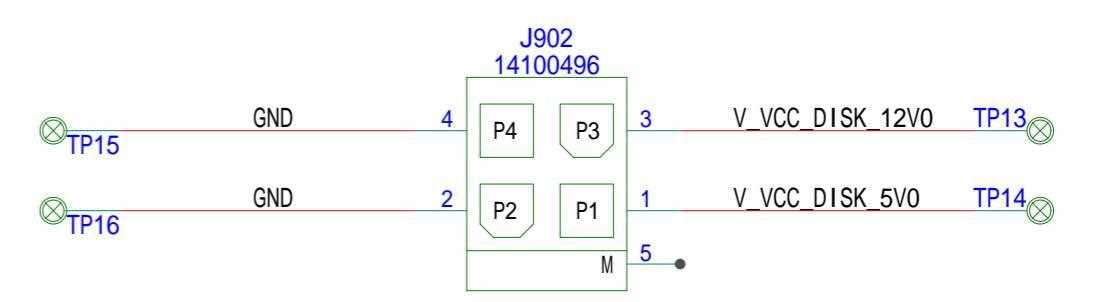




外接SATA硬盘

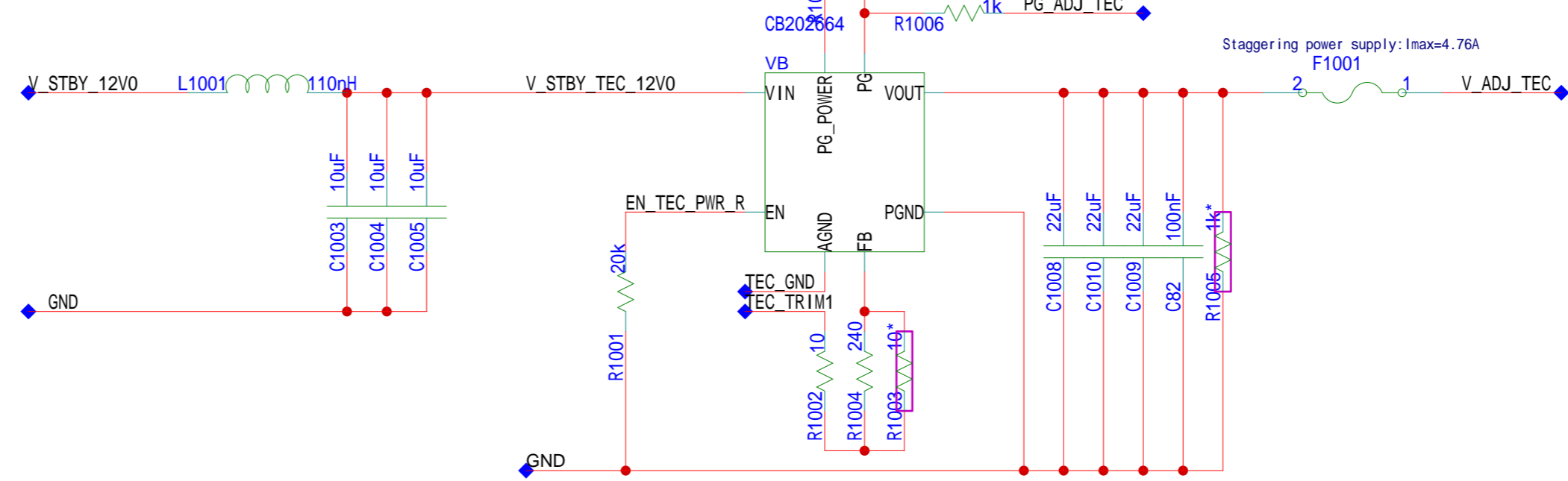
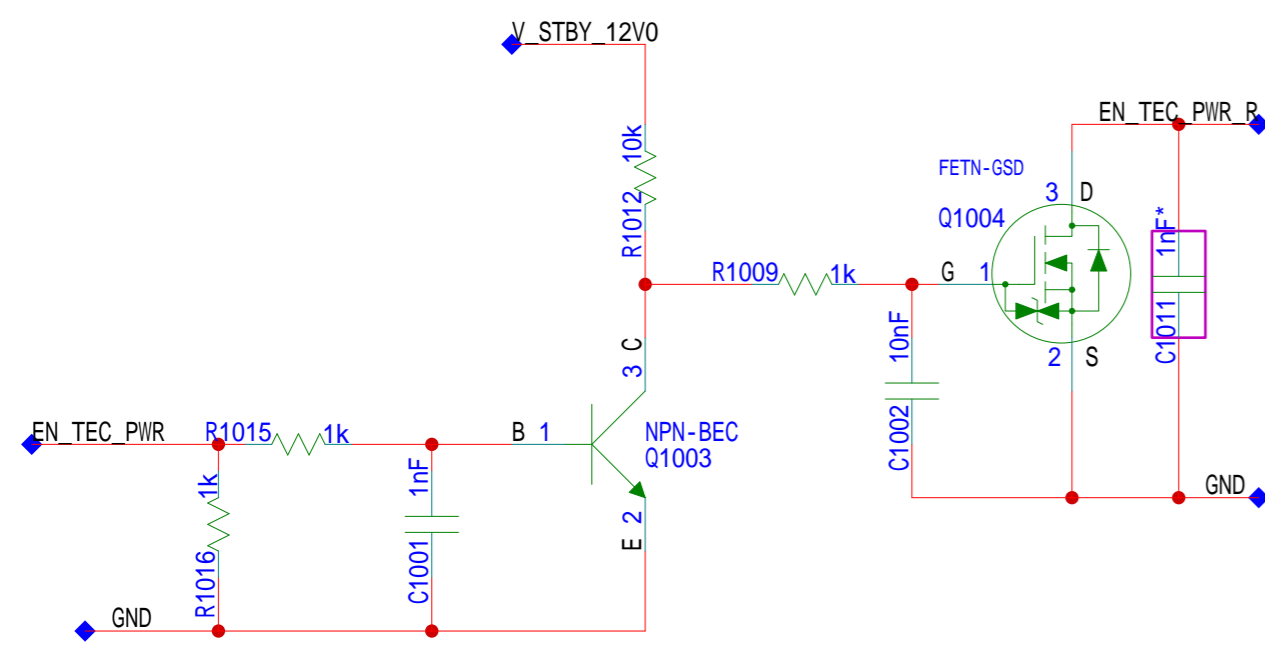


SATA硬盘供电



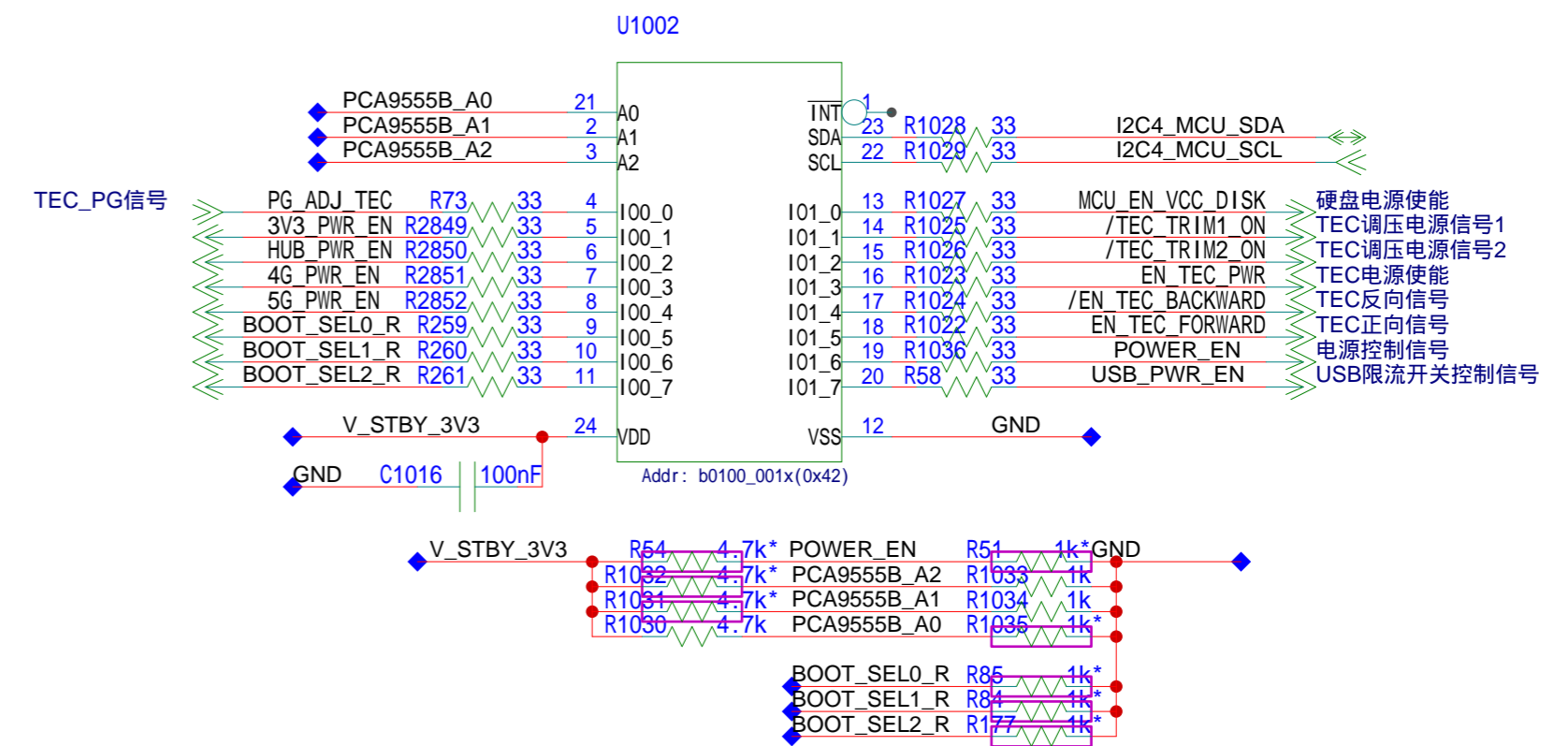
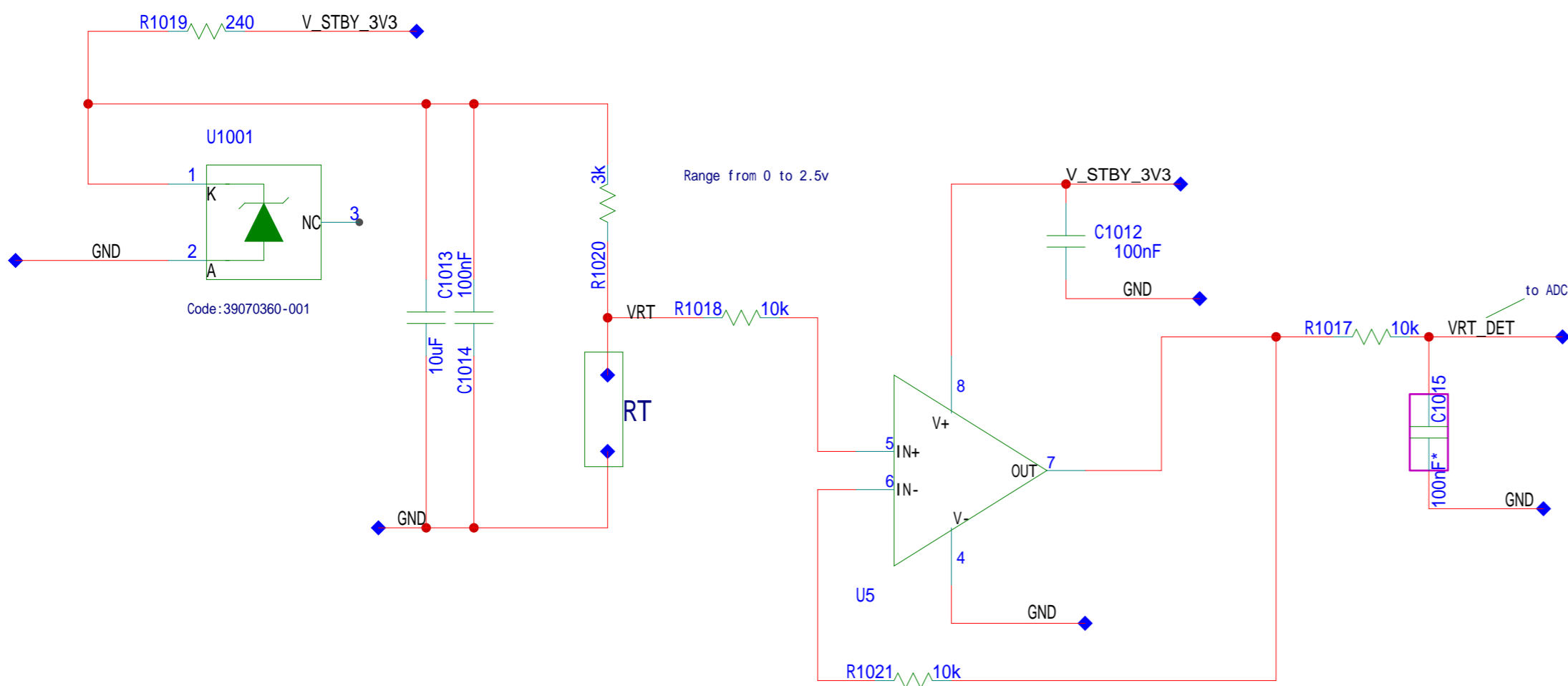
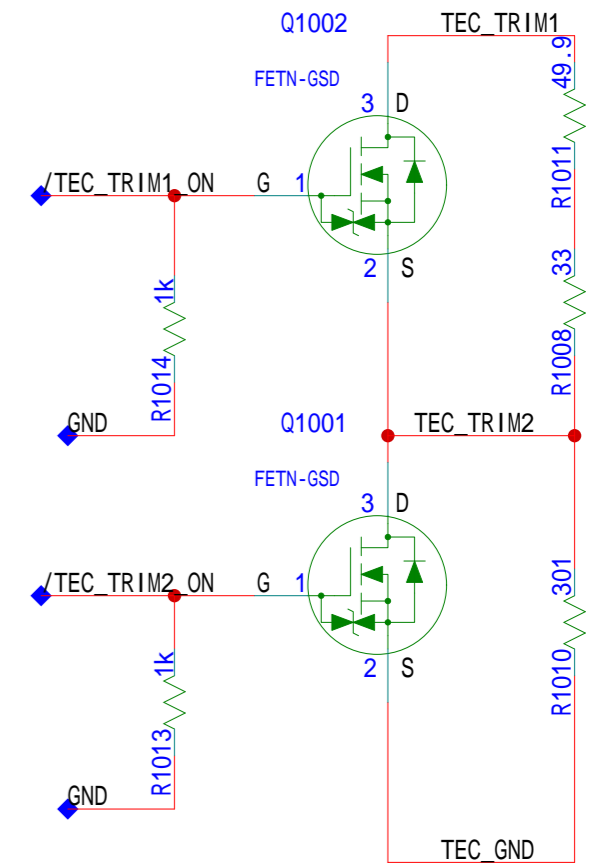
TEC为硬盘加热、降温模块

TEC_POWER

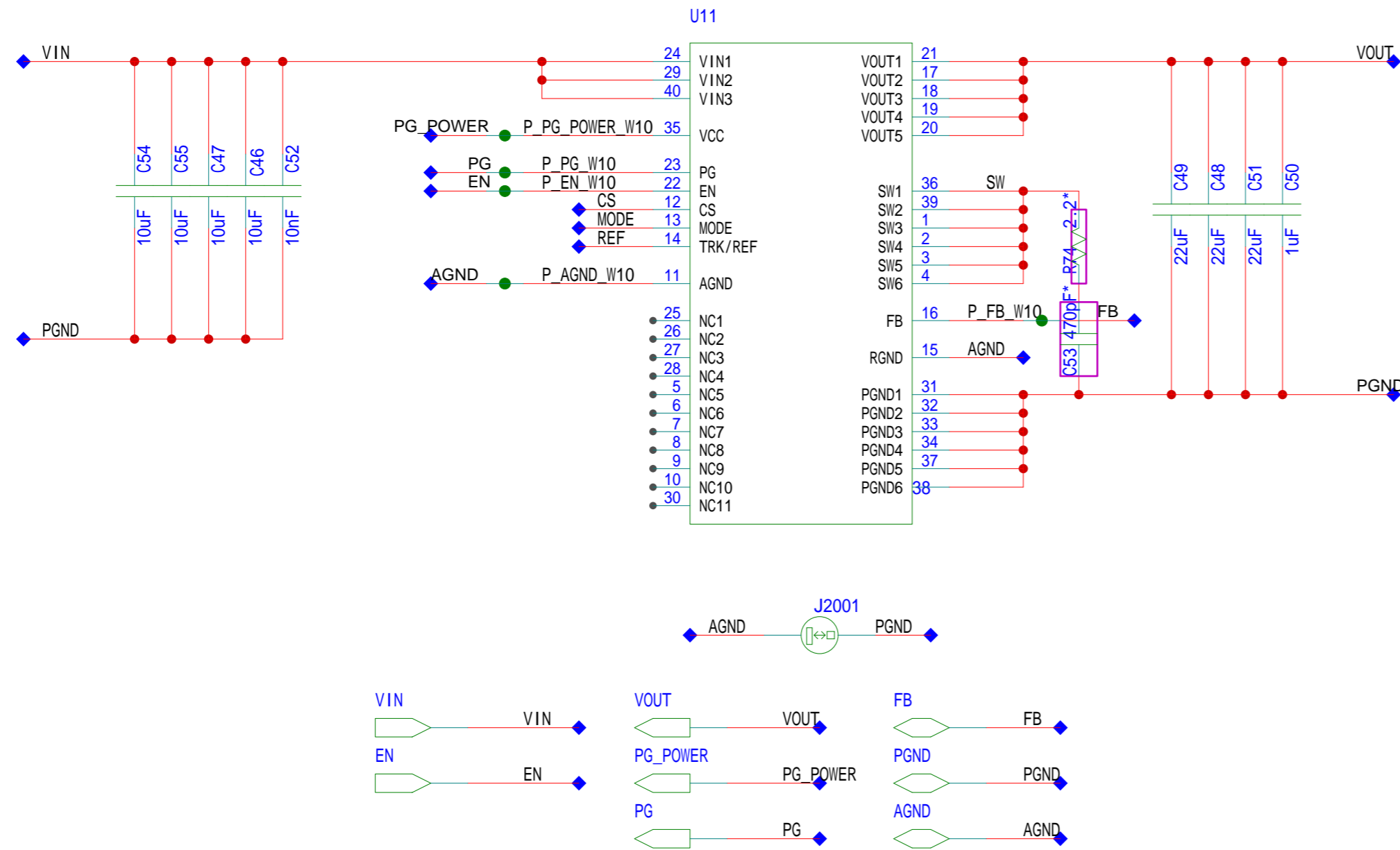


$$V_{out} = 0.6 * (1 + 2/R)$$

/TEC_TRIM1_ON	/TEC_TRIM2_ON	R	VoI
0	0	633.9 Ohm	2.49V
0	1	332.9 Ohm	4.20V
1	1	250 Ohm	5.4V



DC-DC CBB

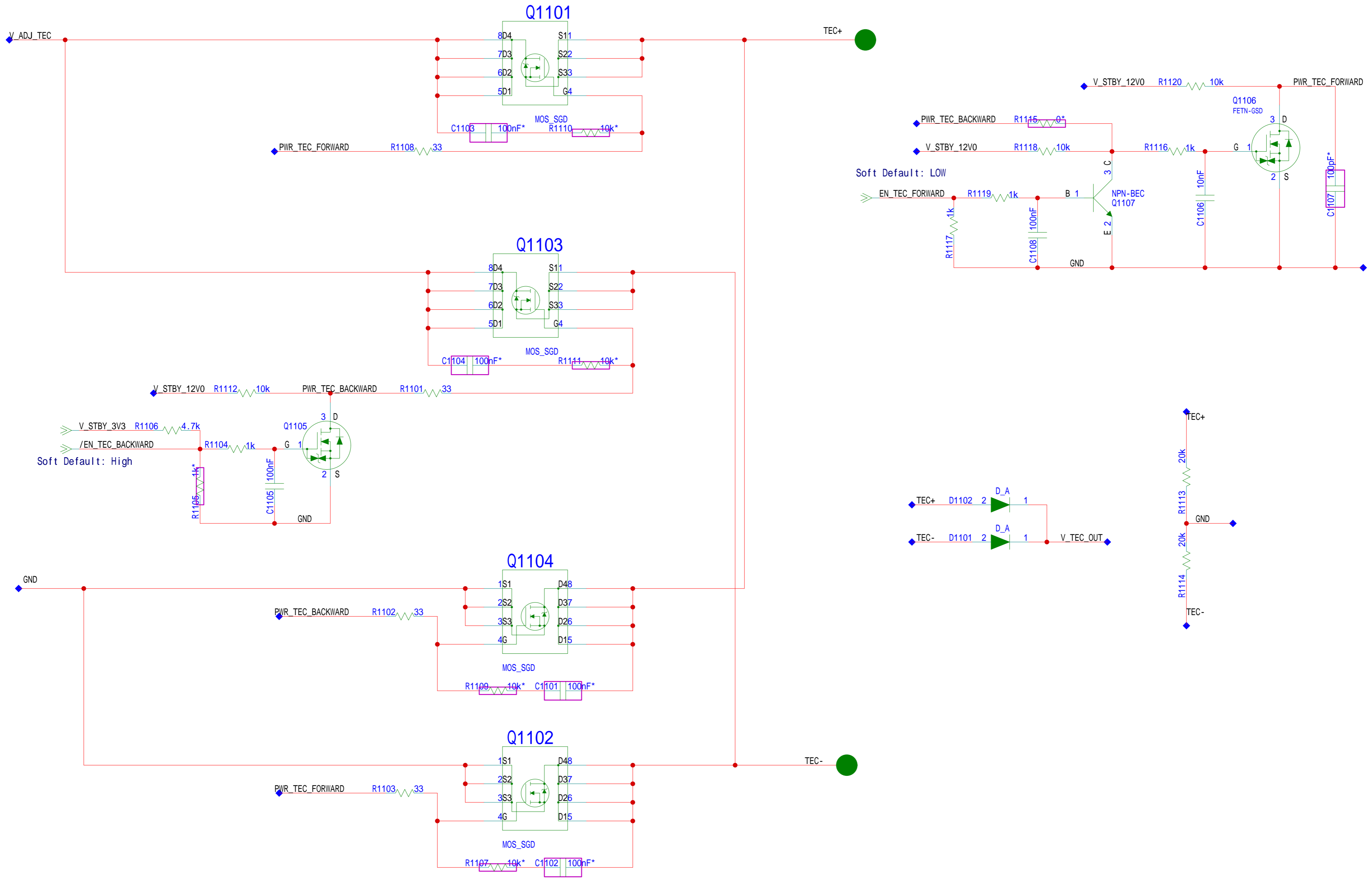


NOTE:详细资料参考应用设计指导书

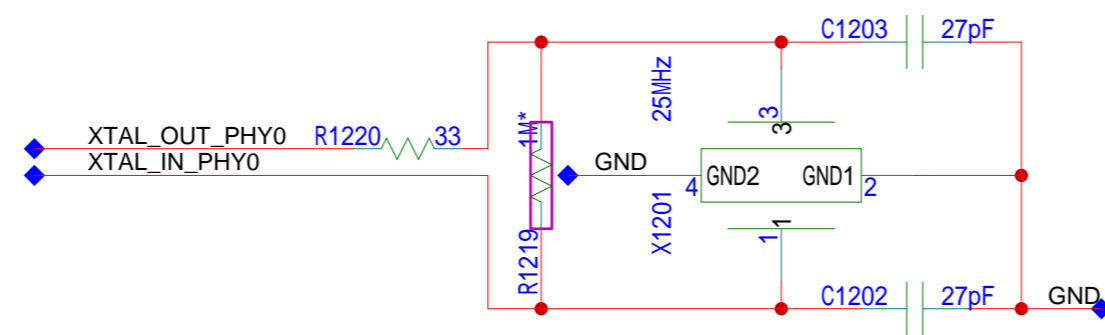
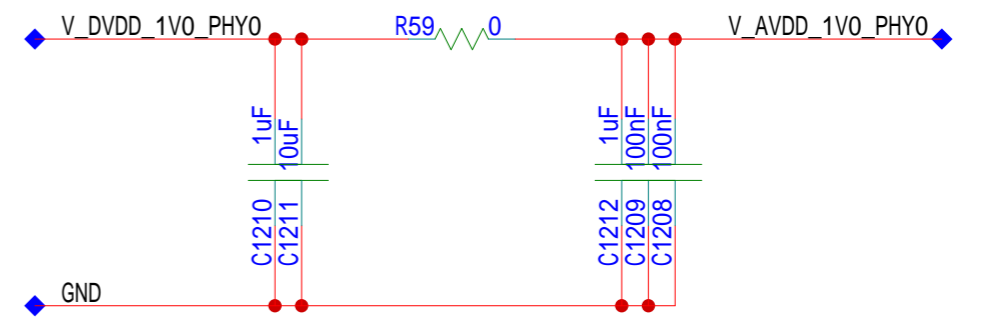
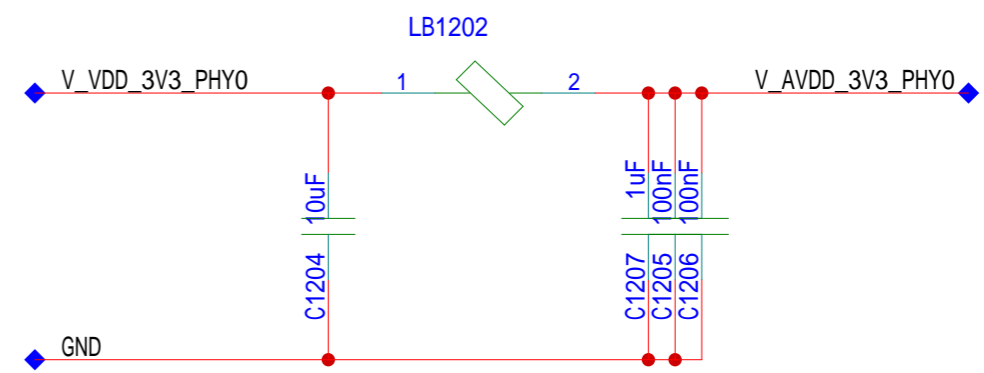
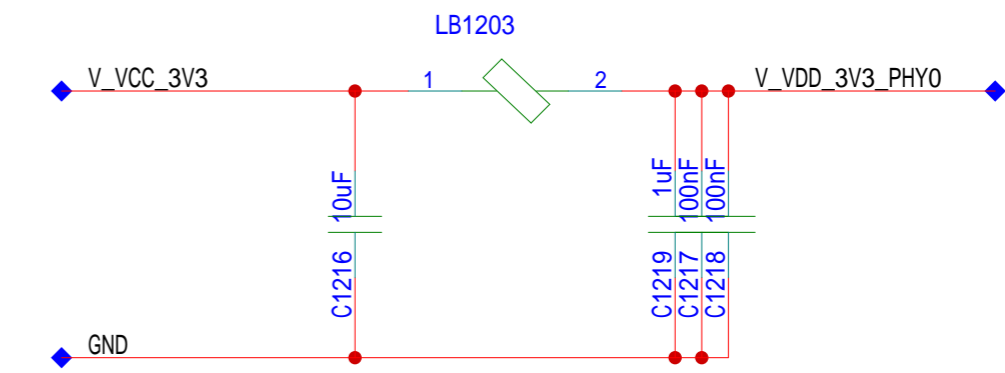
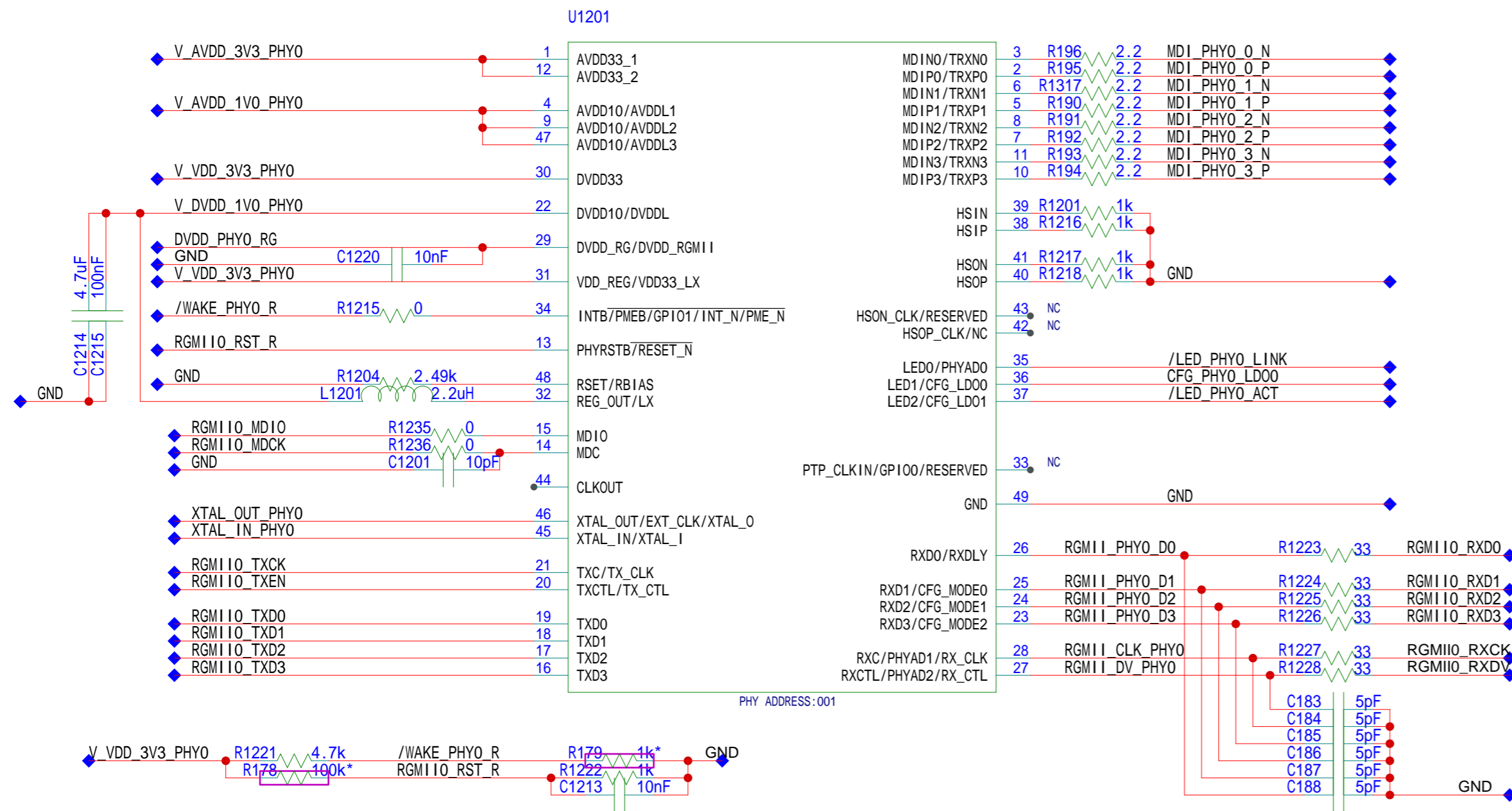
- 1、Vin : Cin最小值为20uF+10nF瓷片电容；
- 2、EN下拉电阻外置；在5V输出及以上场景时，CBB中EN下拉电阻R2001=17.4k（注：如要使用在5V输出以下场景，则需取R2001=20k）；该管脚不要外加电容
- 3、VCC:默认悬空，使用PG时必须上拉到该管脚（3V）
- 4、FB:输出调节，通过FB和RGND之间的电阻来调节输出电压，TRIM调节电阻R1和R2必须选择1%精度电阻。
- 5、PG:不使用PG时悬空，使用时上拉大于等于3K电阻至VCC（3V），且串联一个1K电阻至I/O口，不推荐外部电源（小于3.6V）上拉，外部上拉在EN使能前会有一个0.6V电平；
- 6、MODE:默认悬空，频率设定管脚
- 7、CS:默认悬空，OCP点设定管脚，过流点电阻Rcs（59K）已内置
- 8、Vout : Cout最小值为44uF瓷片电容；
- 9、输出电压与输出电容配置见下表：输出电容选型，请与单板电源工程师讨论

输出电压	0.7V	1.2V	1.8V	3.3V	5.4V
输出电源	9*22UF	7*22UF	5*22UF	4*22UF	3*22UF

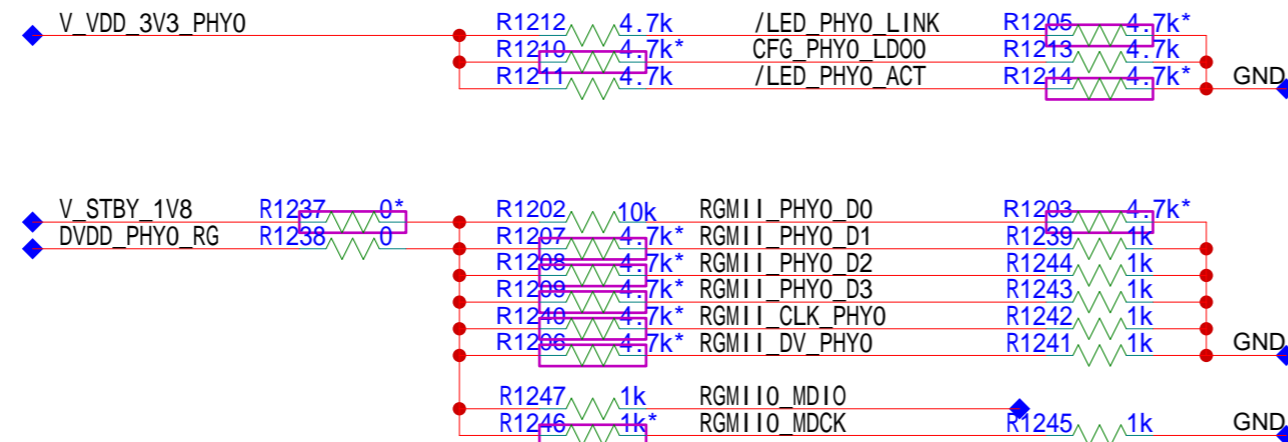
TEC_DRIVER (TEC为硬盘加热、降温模块)



GE PHY



PIN	CFG	PIN	CFG
LED0	PHY_ADD0	RXD1	CFG_MODE0
RXC	PHY_ADD1	RXD2	CFG_MODE1
RXCTL	PHY_ADD2	RXD3	CFG_MODE2
RXD0	RXDLY		
LED1	CFG_LDO(0)		
LED2	CFG_LDO(1)		



10	CFG_LDO(1:0)	LED2 LED1
		STBY_12V0
		01: 2.5V
		10: 1.5V
		11: 1.5V
000	CFG_MODE[2:0]	RXD3 RXD2 RXD1
		000: UTP<->->RGMII
		001: FIBER<->->RGMII
		010: UTP/FIBER<->->RGMII
		011: UTP<->->SGMII
		100: SGMII (PHY)<->->RGMII (MAC)
		101: SGMII (MAC)<->->RGMII (PHY)
		110: UTP<->->FIBER(AUTO MODE)
		111: UTP<->->FIBER(FORCE MODE)
011	PHY_ADD[2:0]	RXCTL RXC LED0
0*		RXDLY

1: add 2ns dly to RXC for RXD 0: no delay

GE SWITCH

1 2 3 4 5 6

A

A

B

B

C

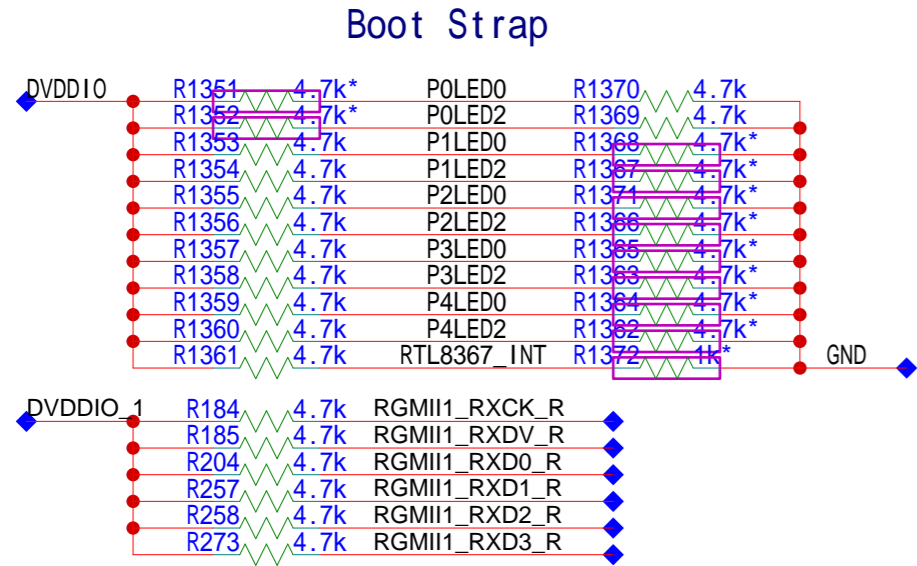
C

D

D

LOOP DETECTION CONFIGURATION
 **PULL UP:DISABLE LOOP DETECTION
 PULL DOWN:ENABLE LOOP DETECTION

INTERRUPT
 ACTIVE LOW BY PULL-UP TO DVDD VIA A 4.7K



POLEDO/SMI_SEL
 PULL UP:EEPROM SMI INTERFACE WHEN DIS_SPIS=1
 **PULL DOWN:MII MANAGEMENT INTERFACE WHEN DIS_SPIS=1

POLED2/EN_PHY
 **PULL UP:ENABLE EMBEDDED PHY
 PULL DOWN:DISABLE EMBEDDED PHY

P1LED0/MIDO
 PULL UP:MII PHY MANAGEMENT INTERFACE ID IS 29
 **PULL DOWN:MII PHY MANAGEMENT INTERFACE ID IS 0

P1LED2/RESERVED
 **MUST PULL HIGH OR KEEP FLOATING

P2LED0/DISAUTOLOAD
 **PULL UP:DISABLE EEPROM AUTOLOAD
 PULL DOWN:ENABLE EEPROM AUTOLOAD

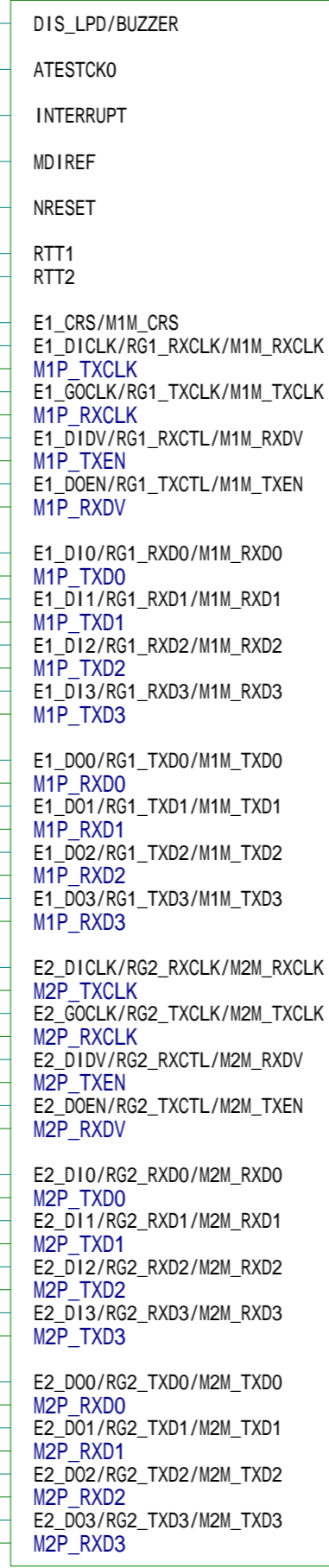
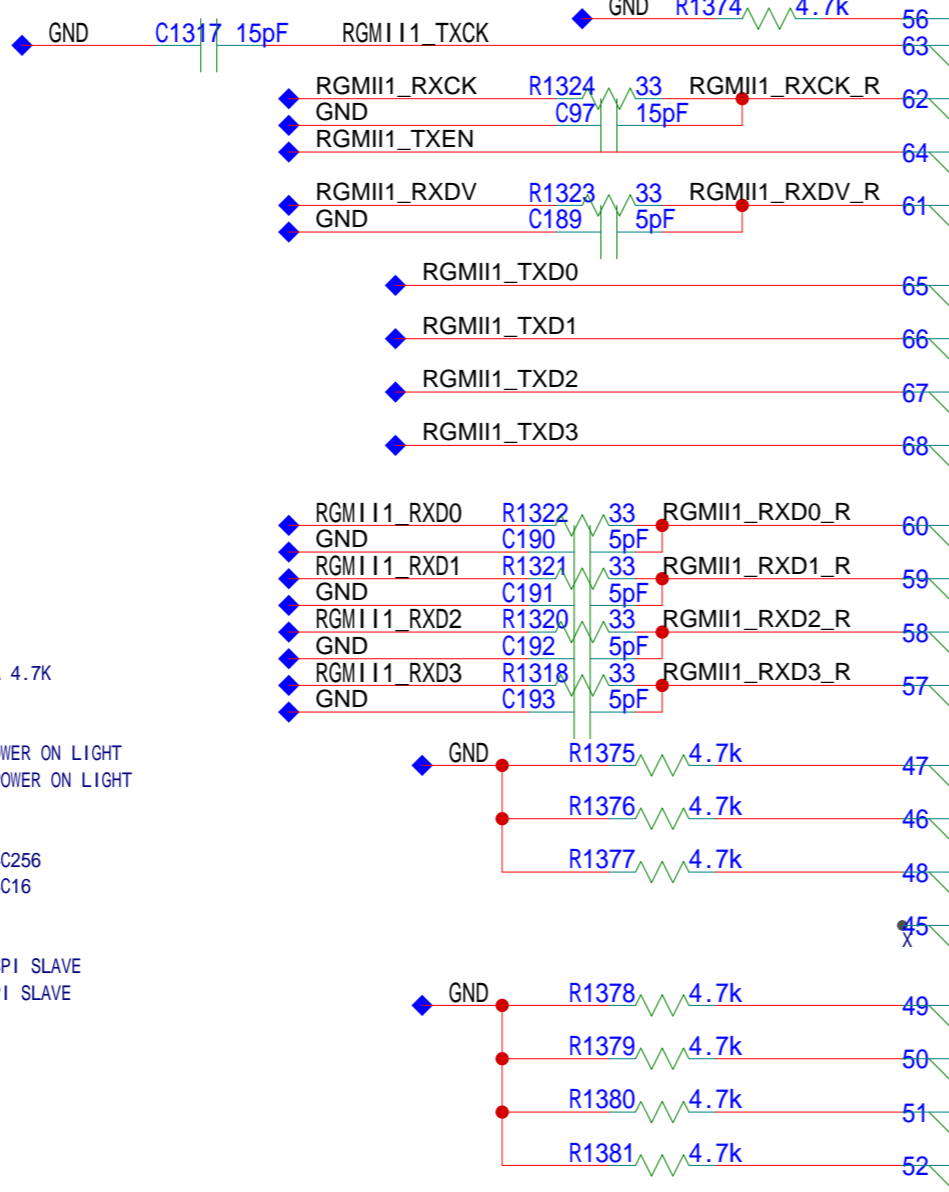
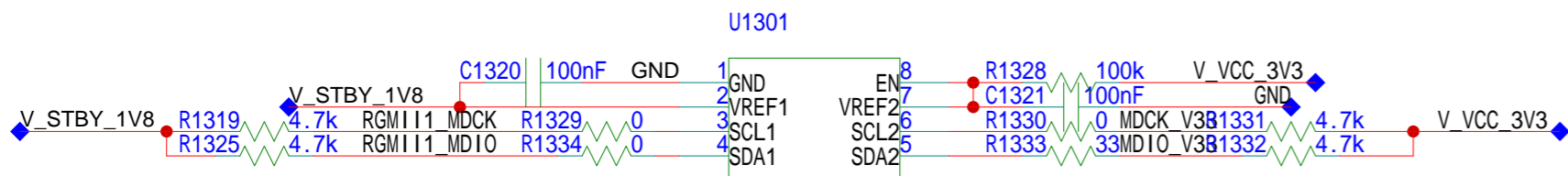
P2LED2/DIS_8051
 **PULL UP:DISABLE 8051
 PULL DOWN:ENABLE 8051

P3LED0/RESERVED
 **MUST PULL LOW VIA 4.7K

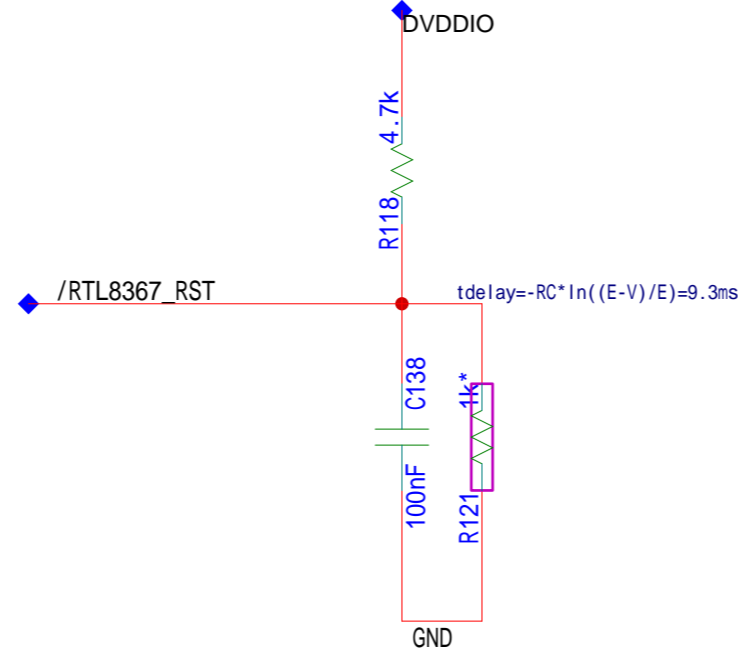
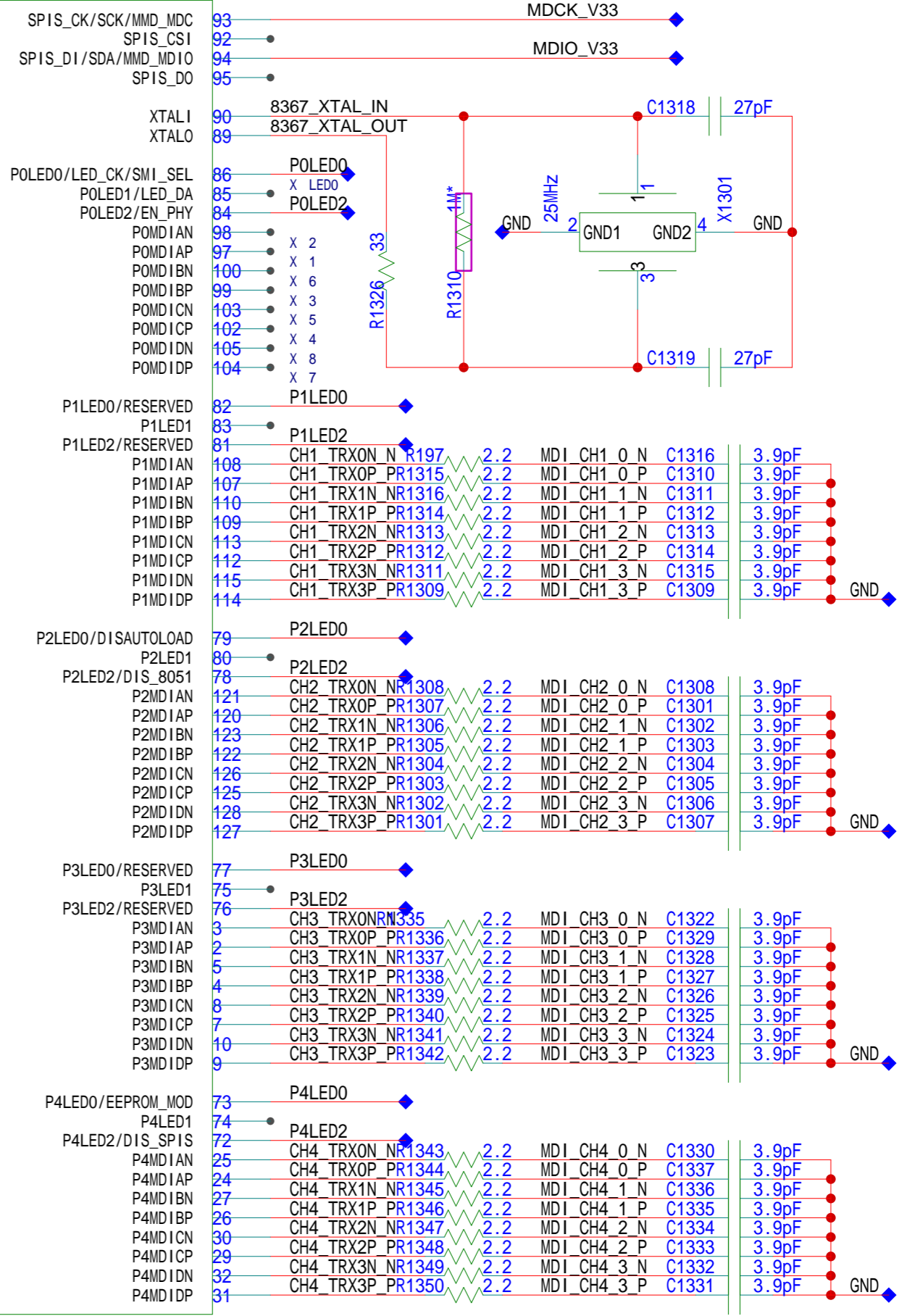
P3LED2/EN_PWRLIGHT
 **PULL UP:ENABLE POWER ON LIGHT
 PULL DOWN:DISABLE POWER ON LIGHT

P4LED0/EEPROM_MOD
 **PULL UP:24C32--24C256
 PULL DOWN:24C02--24C16

P4LED2/DIS_SPI
 **PULL UP:DISABLE SPI SLAVE
 PULL DOWN:ENABLE SPI SLAVE

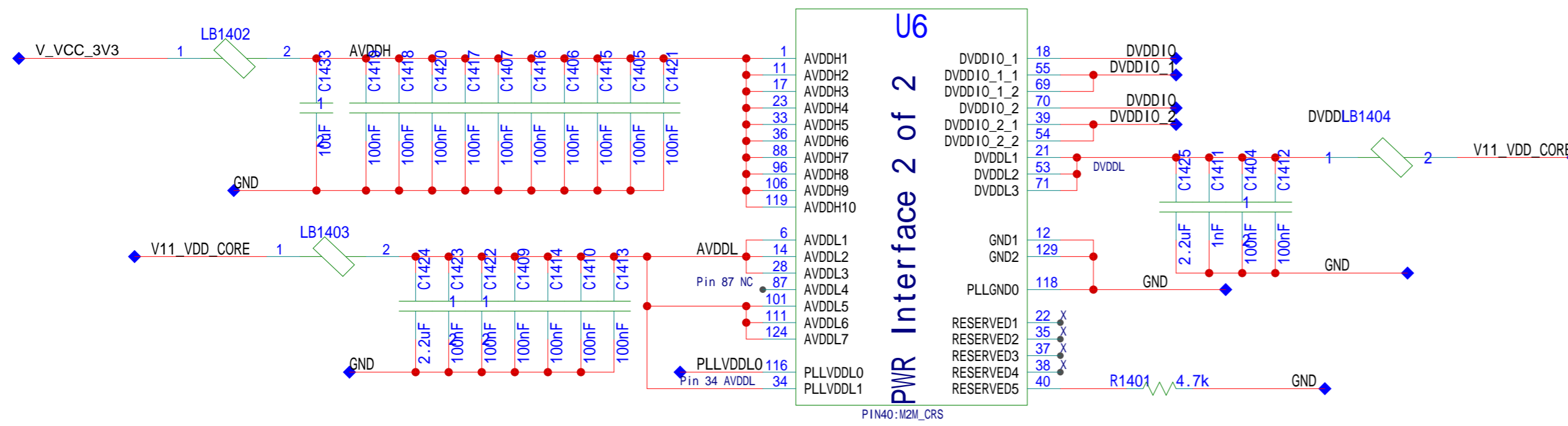


U6
 MISC Interface 1 of 2



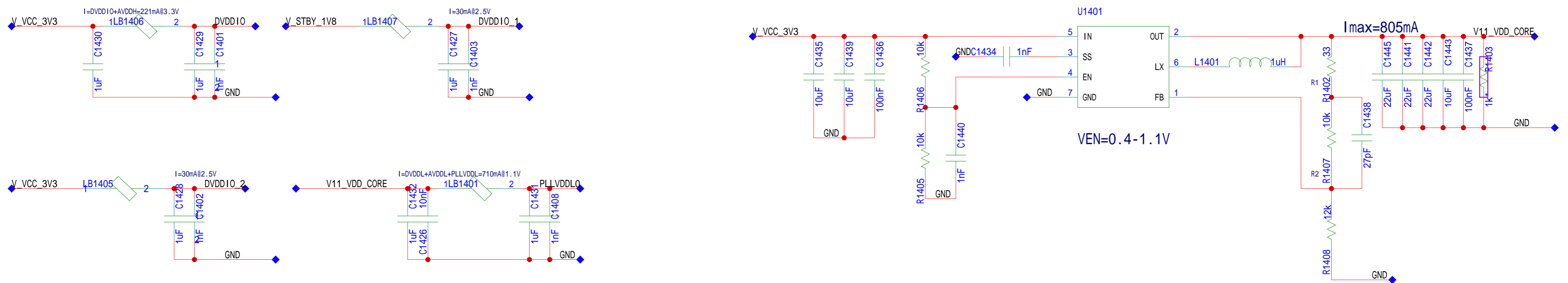
1 2 3 4 5 6

GE SWITCH PWR



DC/DC V33->V11_VDD_CORE

$$V_{out} = V_{REF} * (1 + R1/R2) = 0.6 * (1 + 10/12) = 1.1V$$



A

A

B

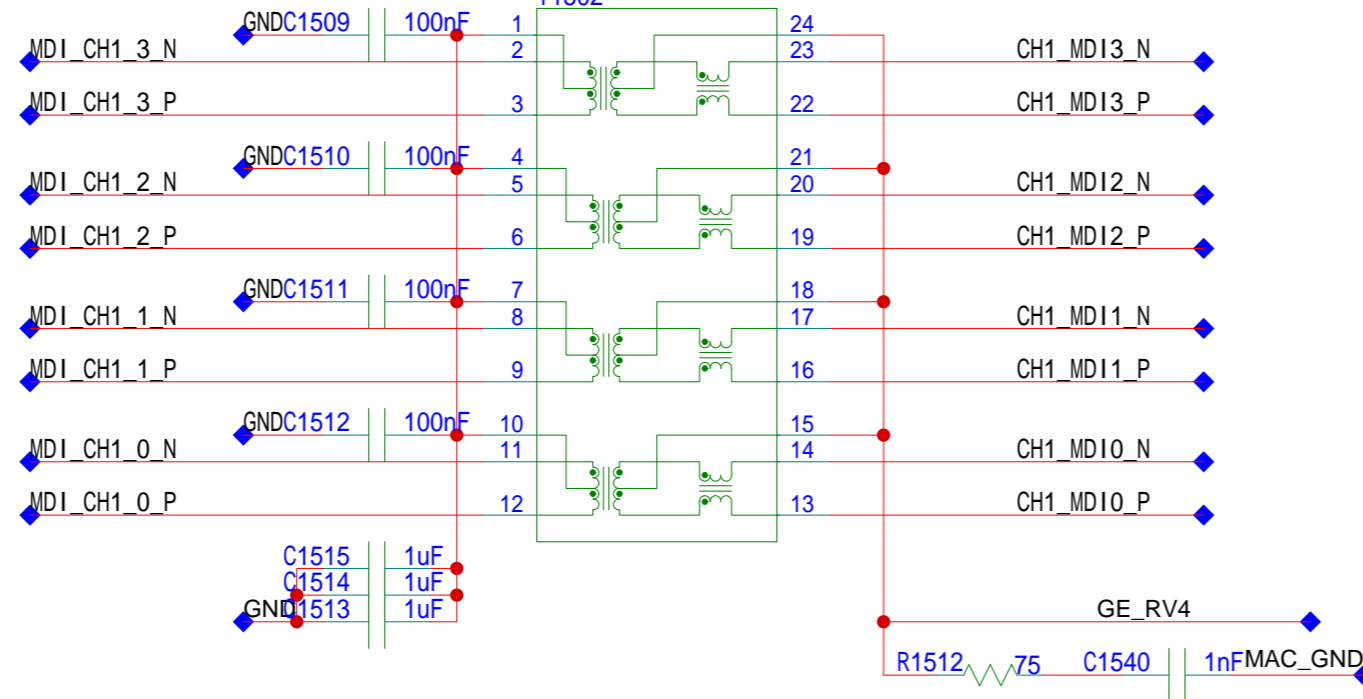
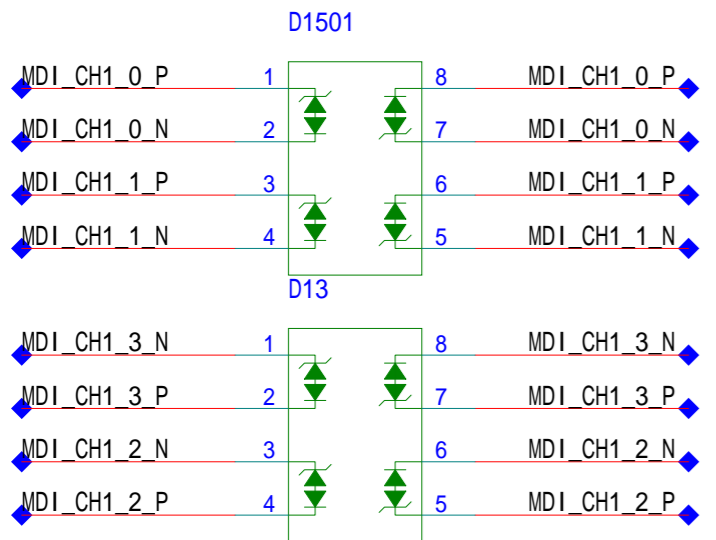
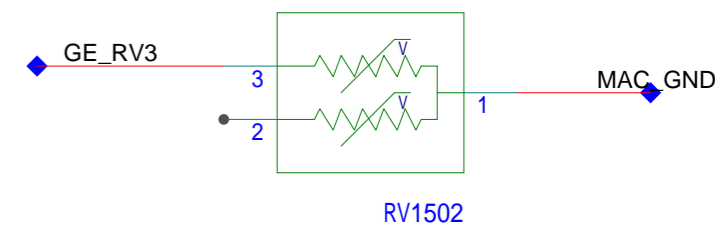
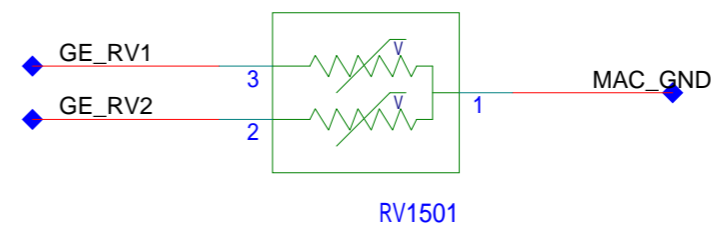
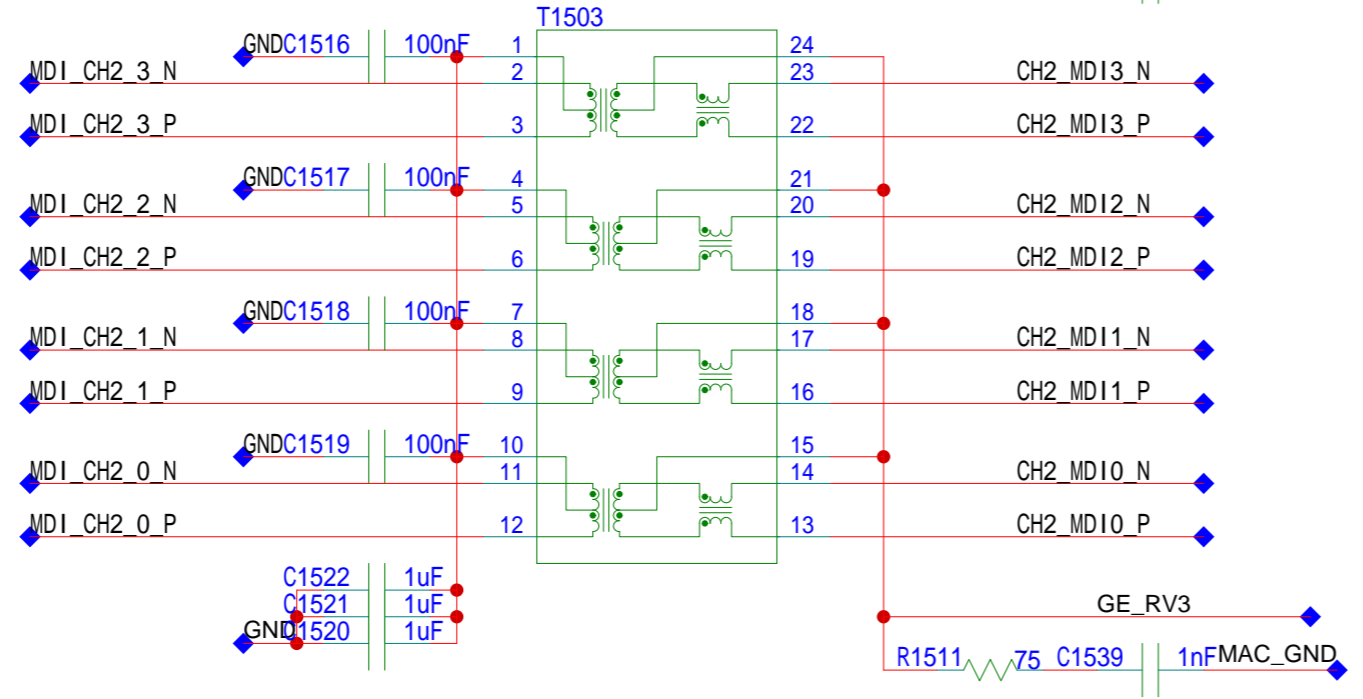
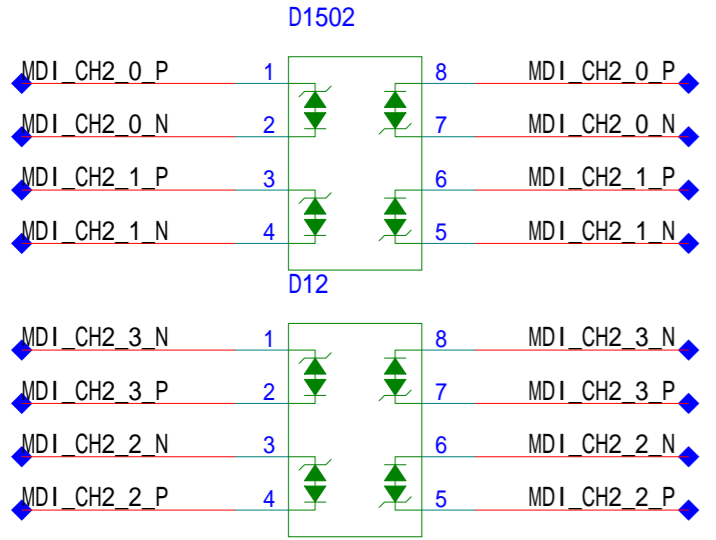
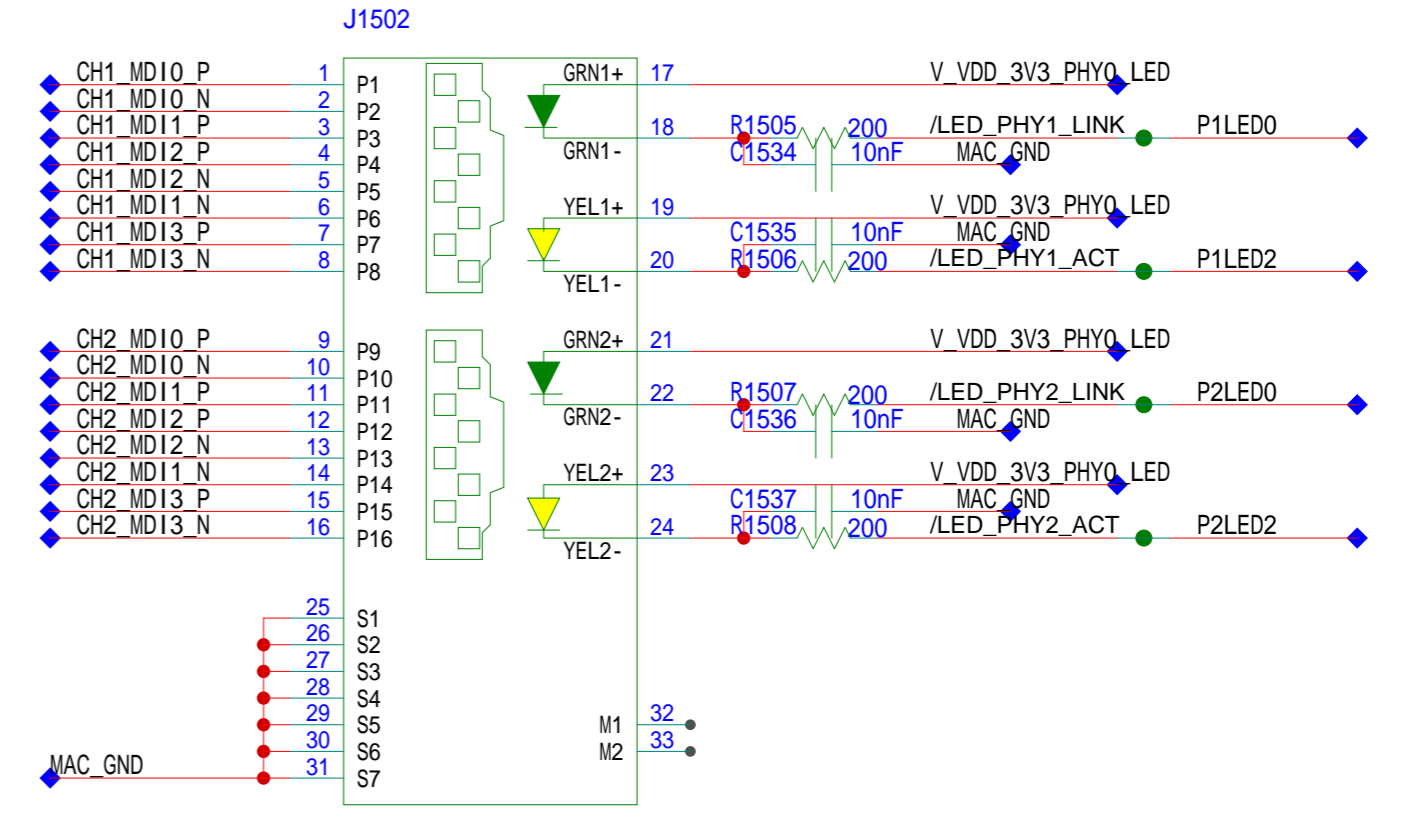
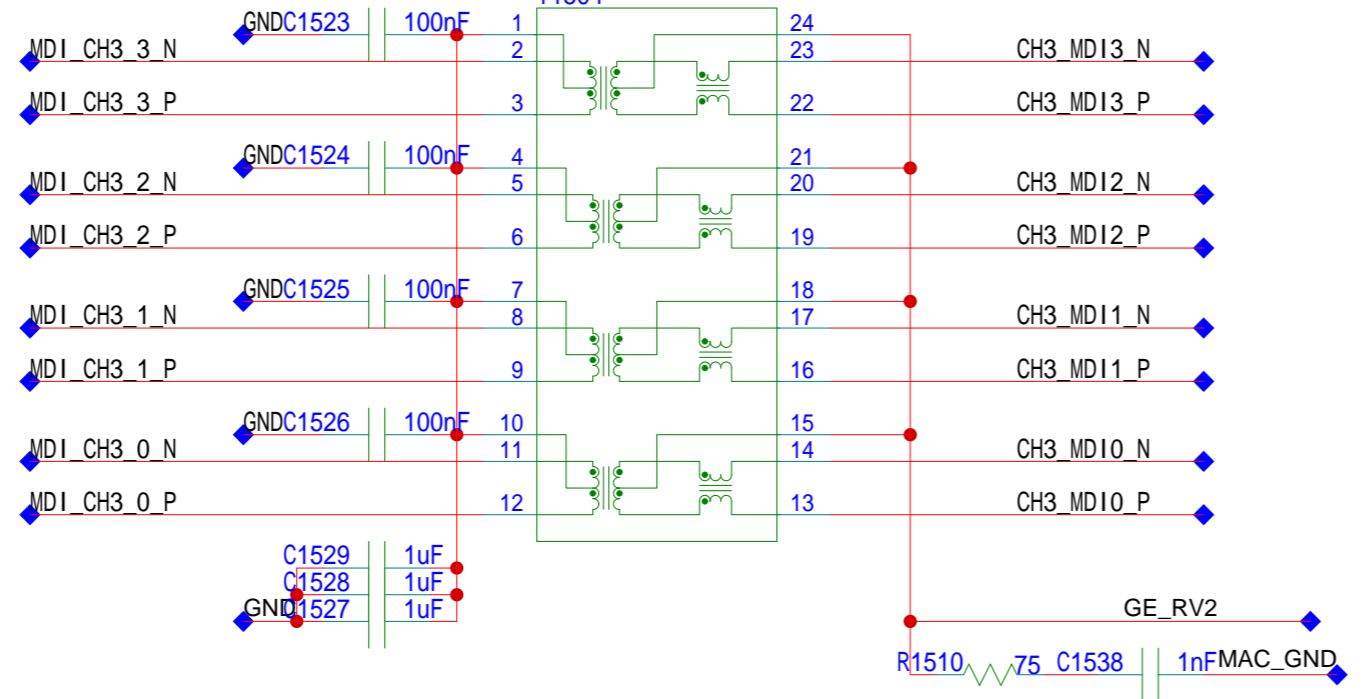
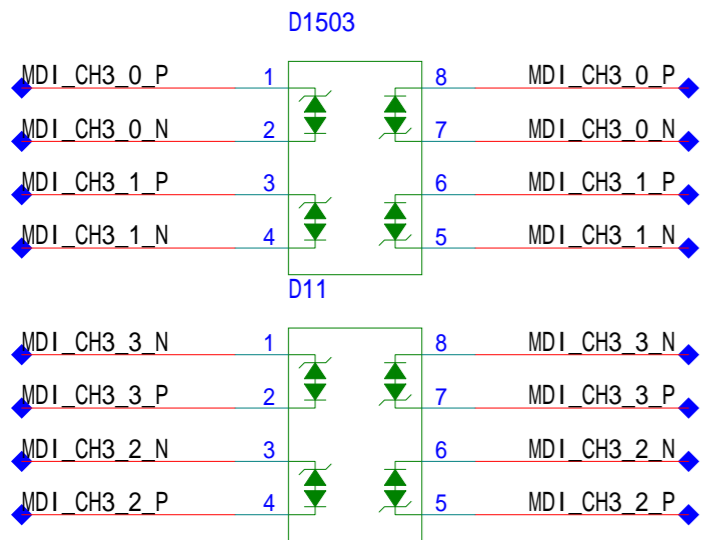
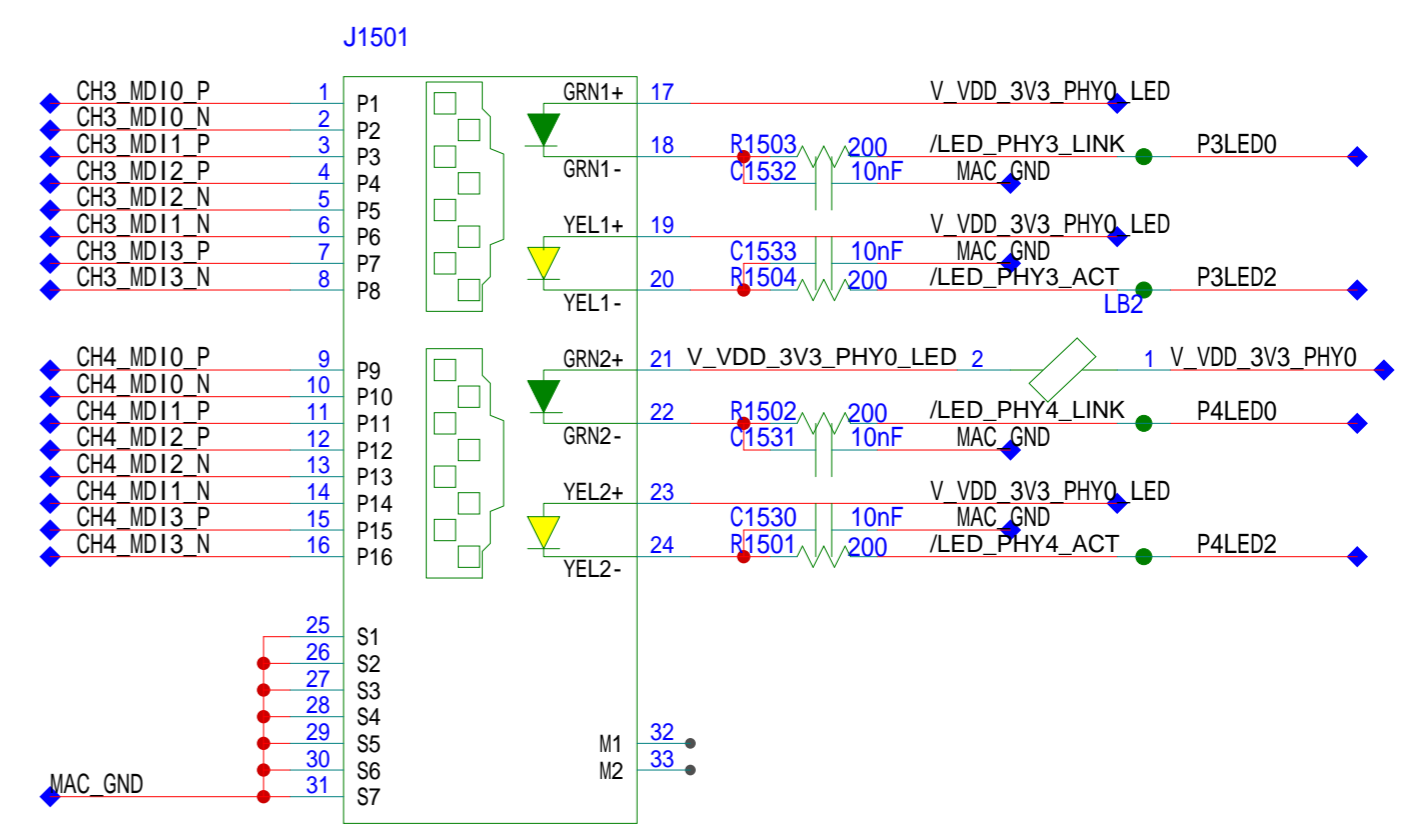
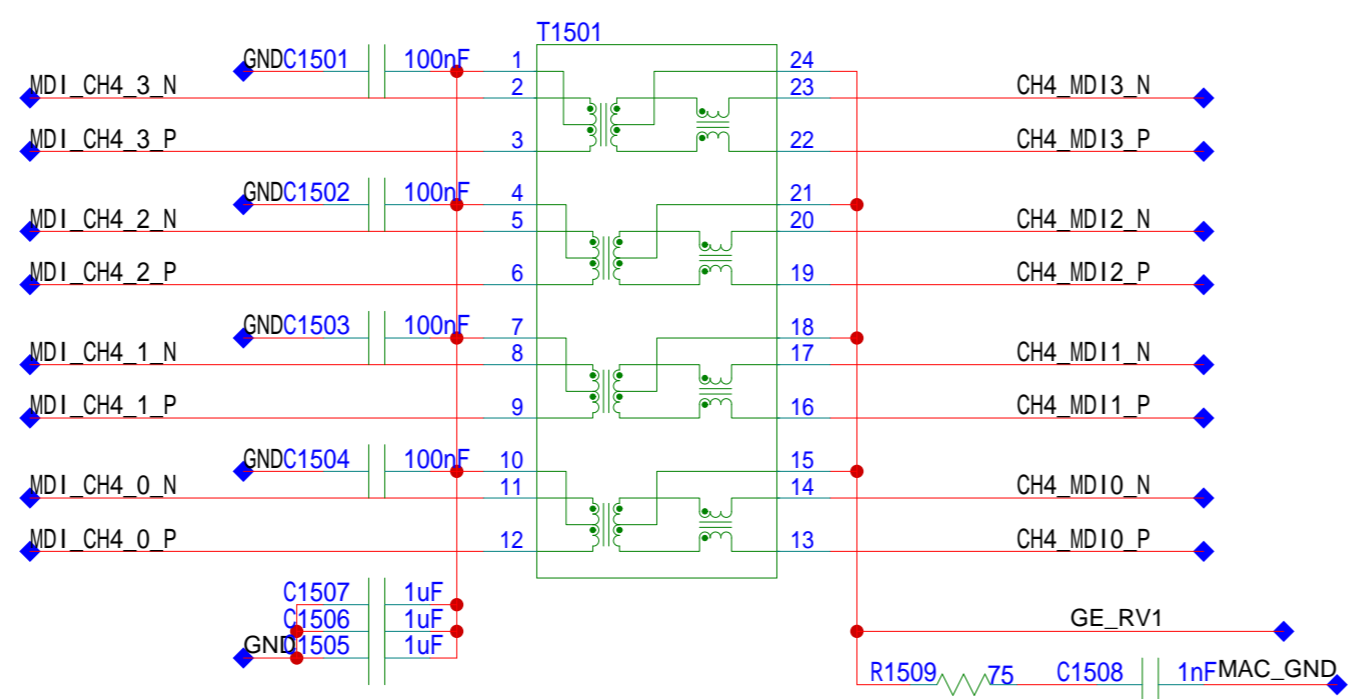
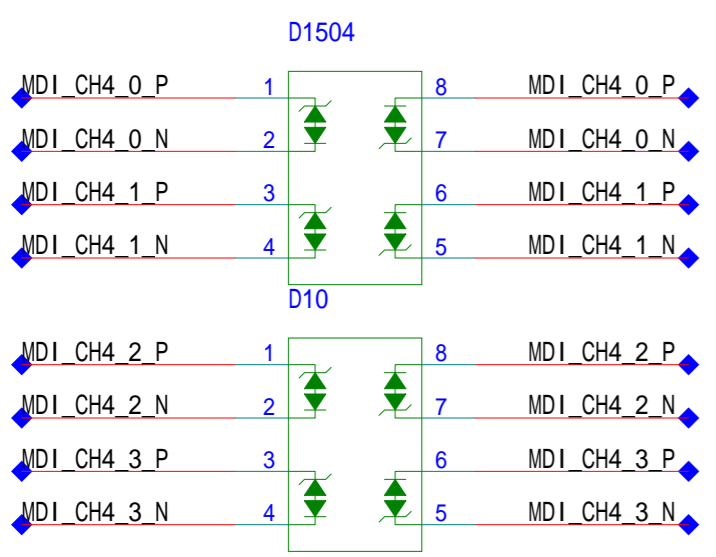
B

C

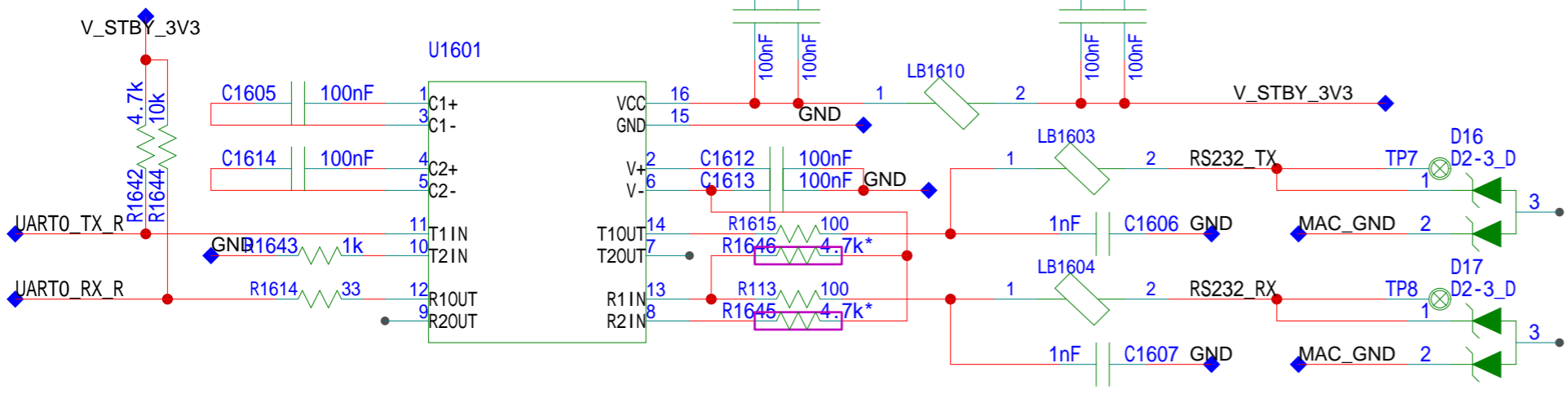
C

D

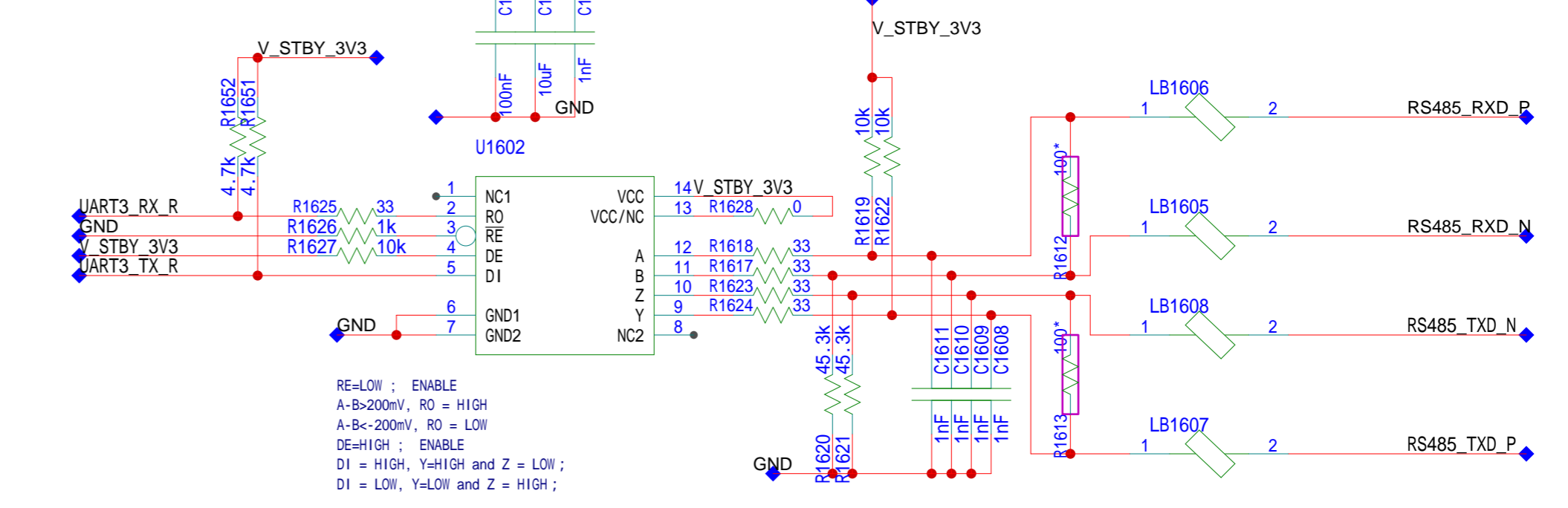
D



RS232

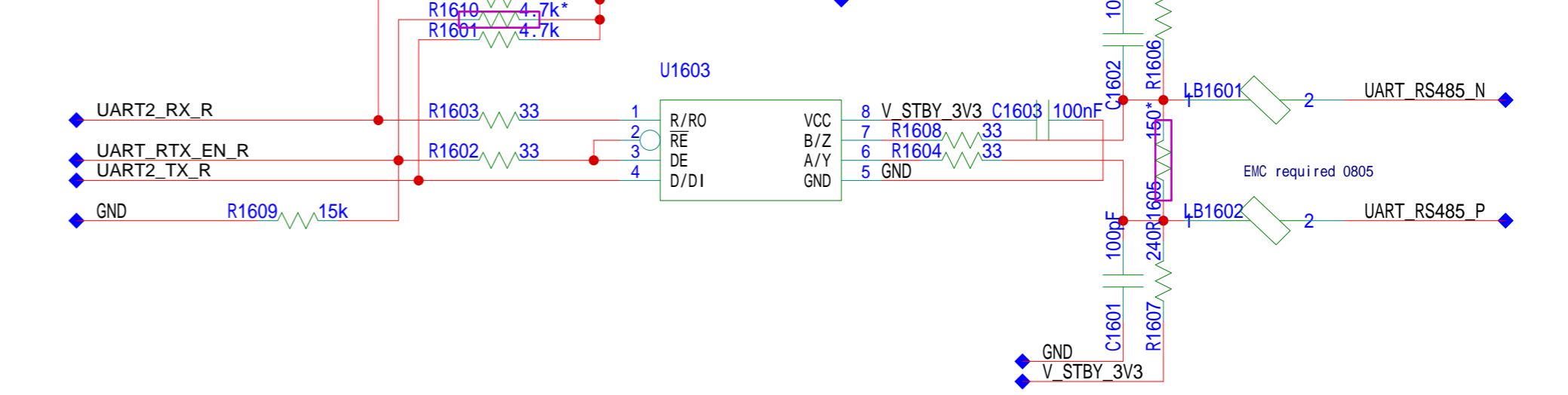


RS485全双工

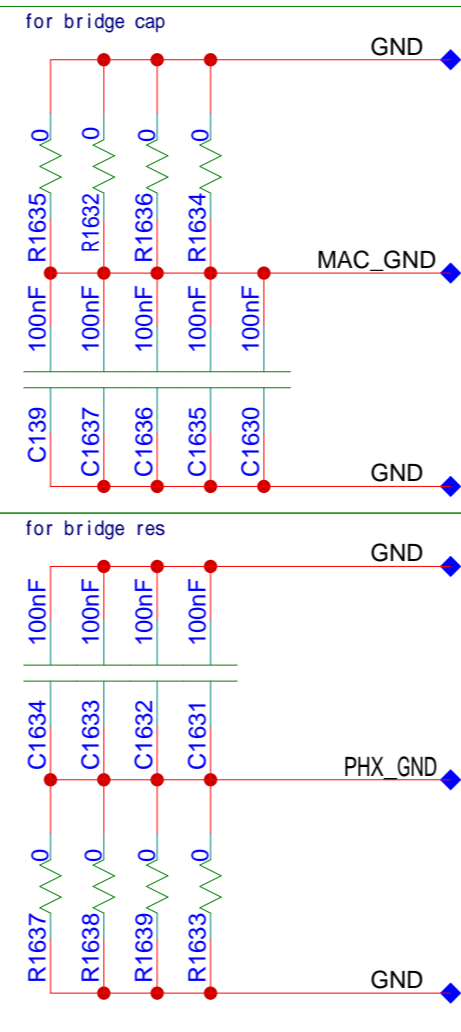
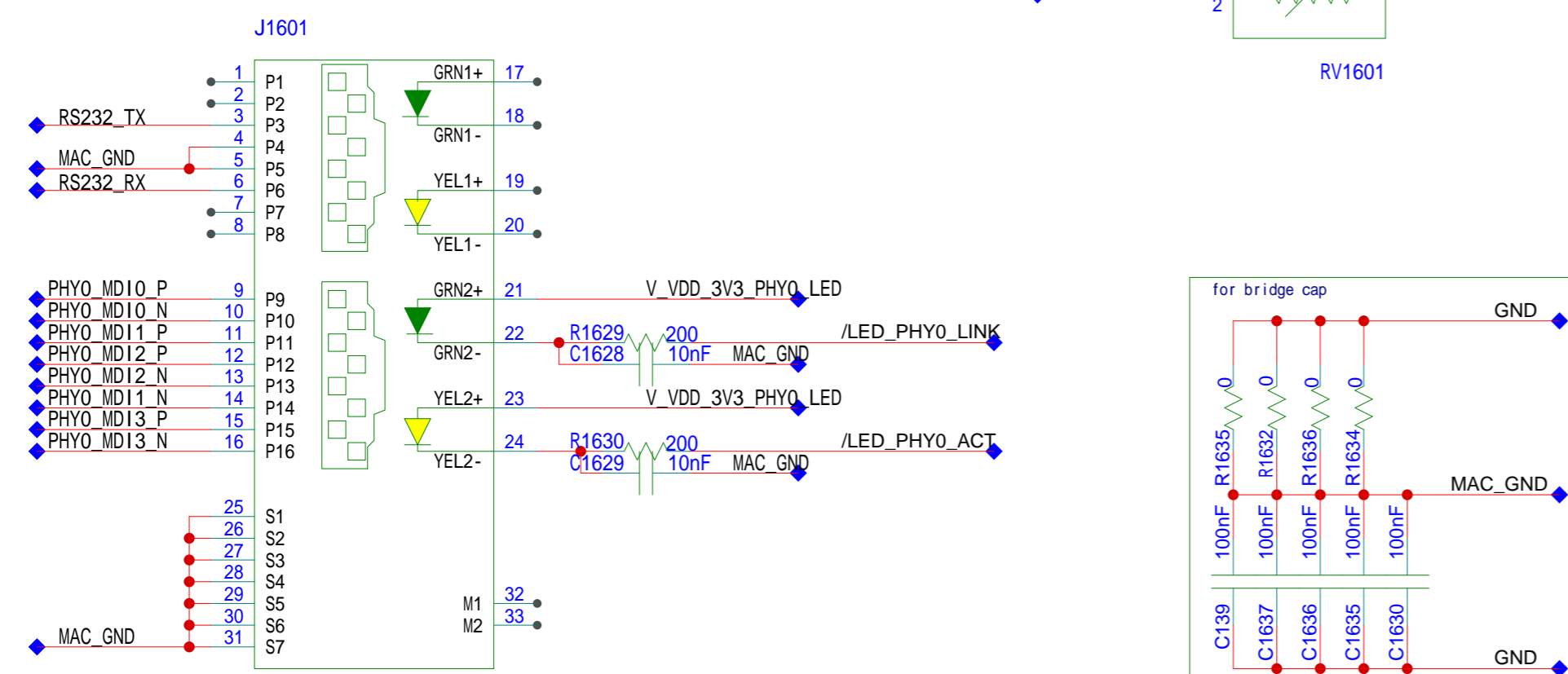
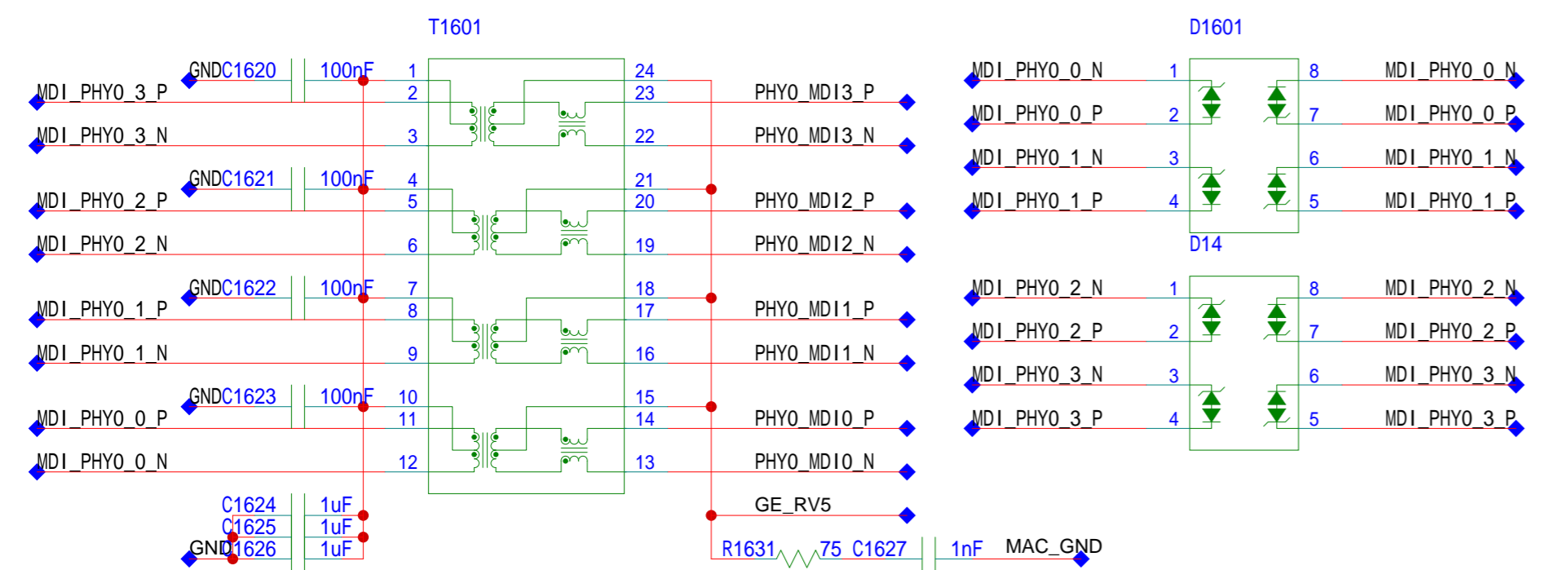
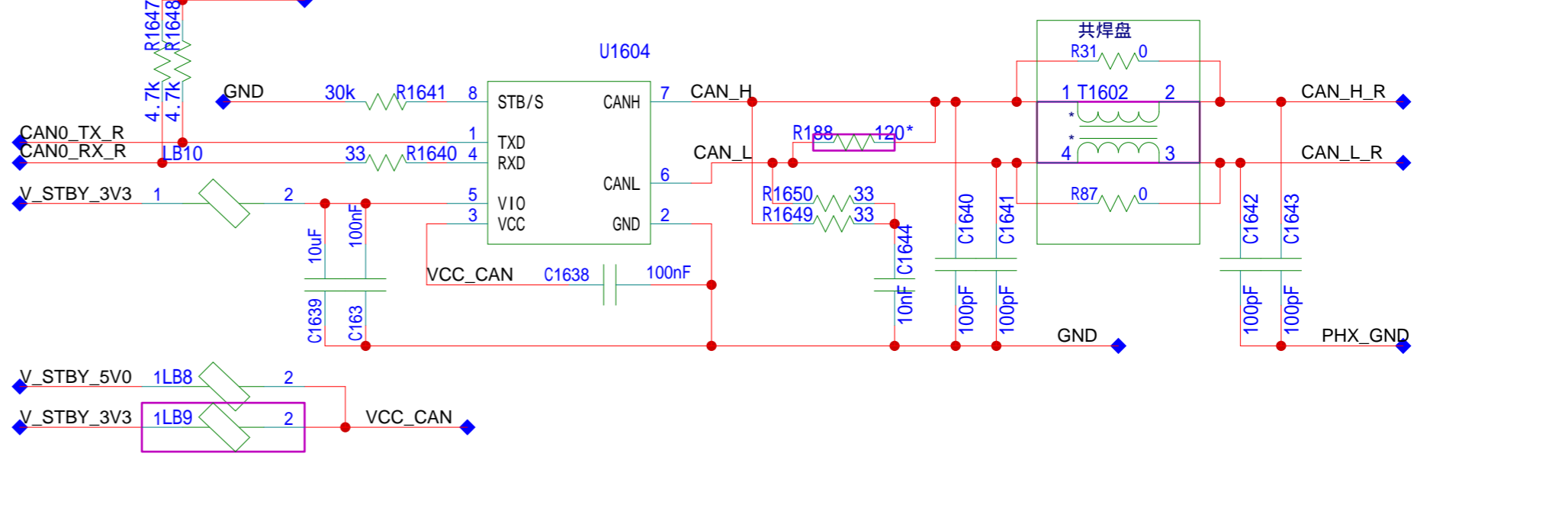


RE=LOW ; ENABLE
A-B>200mV, RO = HIGH
A-B<200mV, RO = LOW
DE=HIGH ; ENABLE
DI = HIGH, Y=HIGH and Z = LOW ;
DI = LOW, Y=LOW and Z = HIGH ;

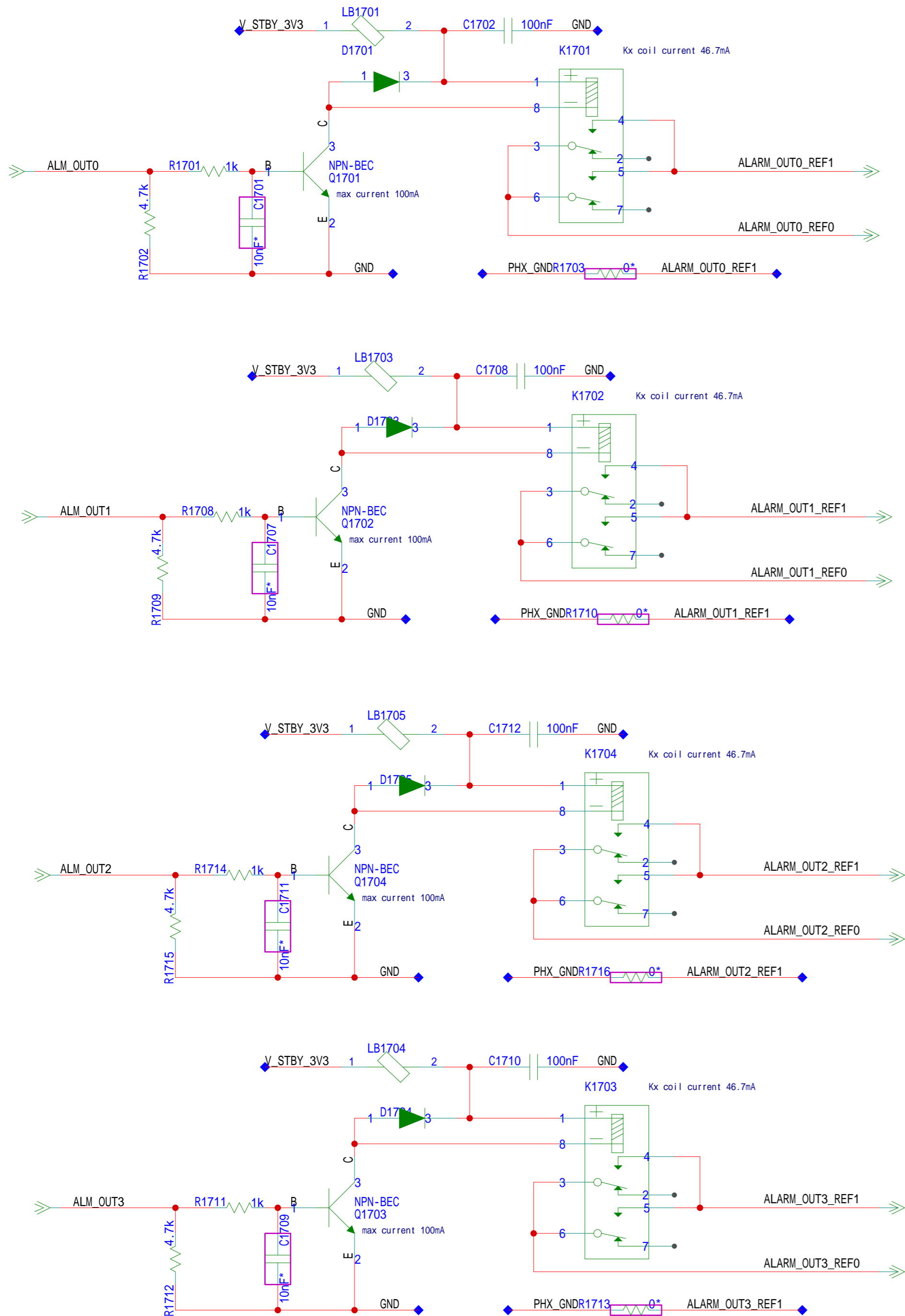
RS485半双工



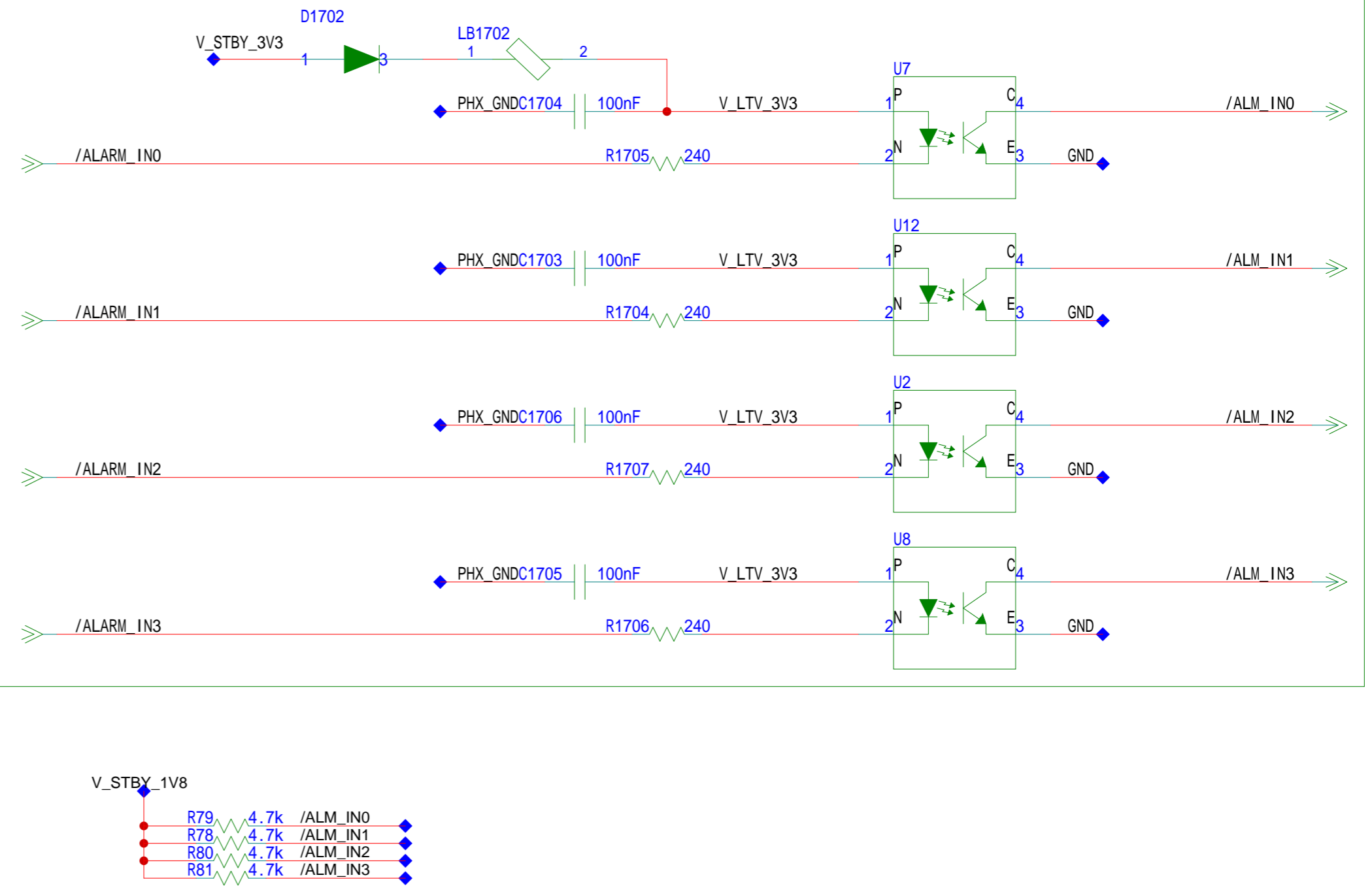
CAN



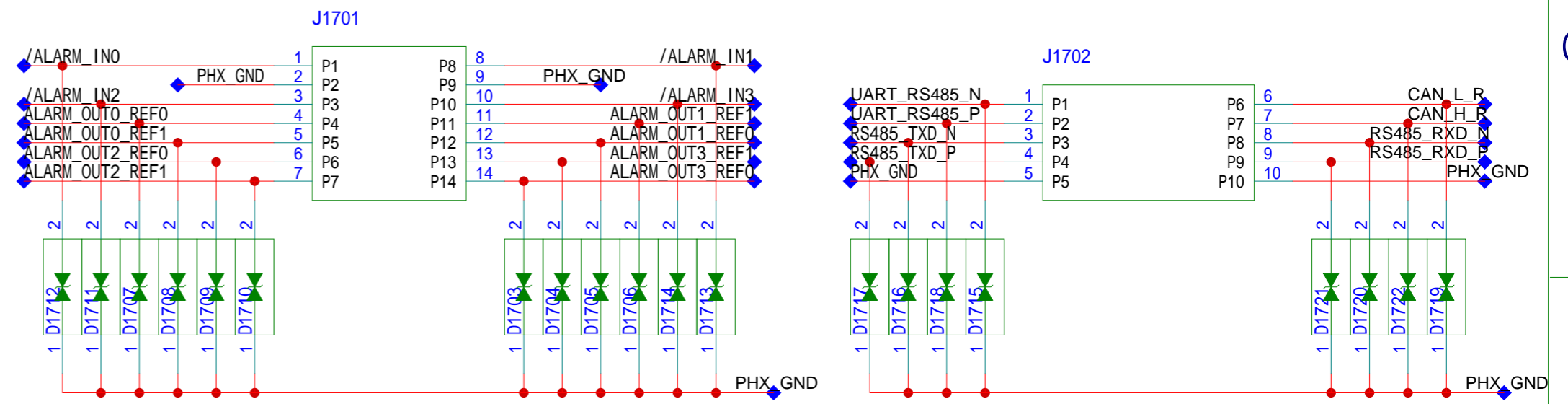
ALARM 4 OUT



ALARM 4 IN



PHOENIX



EMMC

EMMC_DATA0	R1825	10	EMMC_DATA0_R	A3
EMMC_DATA1	R1826	10	EMMC_DATA1_R	A4
EMMC_DATA2	R1827	10	EMMC_DATA2_R	A5
EMMC_DATA3	R1828	10	EMMC_DATA3_R	B2
EMMC_DATA4	R1829	10	EMMC_DATA4_R	B3
EMMC_DATA5	R1830	10	EMMC_DATA5_R	B4
EMMC_DATA6	R1831	10	EMMC_DATA6_R	B5
EMMC_DATA7	R1832	10	EMMC_DATA7_R	B6

DAT0	A3
DAT1	A4
DAT2	A5
DAT3	B2
DAT4	B3
DAT5	B4
DAT6	B5
DAT7	B6

EMMC_DS	R1807	33	H5	DS
EMMC_CLK	R1808	33	M6	CLK
GND	C1811	22pF*		
EMMC_CMD	R114	33	M5	CMD

V_VCC_1V8_EMMC	R1810	4.7k	K5	RST_N/RSTN
GND	C1812	10nF		

A6	VSS1
E7	VSS2
G5	VSS3
H10	VSS4
J5	VSS5
K8	VSS6
C4	VSSQ1
N2	VSSQ2
N5	VSSQ3
P4	VSSQ4
P6	VSSQ5

MISC Interface 1 of 2

RFU1	A7
RFU2	E5
RFU3	K6
RFU4	K7
RFU/VSF1	E8
RFU/VSF2	E9
RFU/VSF3	F10
RFU/VSF4	G10
RFU/VSF5	K10
RFU/VSF6	P10
RFU/VSF7	P10

VCC1	E6	V_VCC_3V3_EMMC	
VCC2	F5	C1818	10uF
VCC3	J10	C1819	100nF
VCC4	K9	C1820	100nF
GND			

VCCQ1	C6	C1821	10uF	V_VCC_1V8_EMMC
VCCQ2	M4	C1822	100nF	
VCCQ3	N4	C1822	100nF	
VCCQ4	P3	C1823	100nF	GND
VCCQ5	P5			

NC/INDEX	D4	GND
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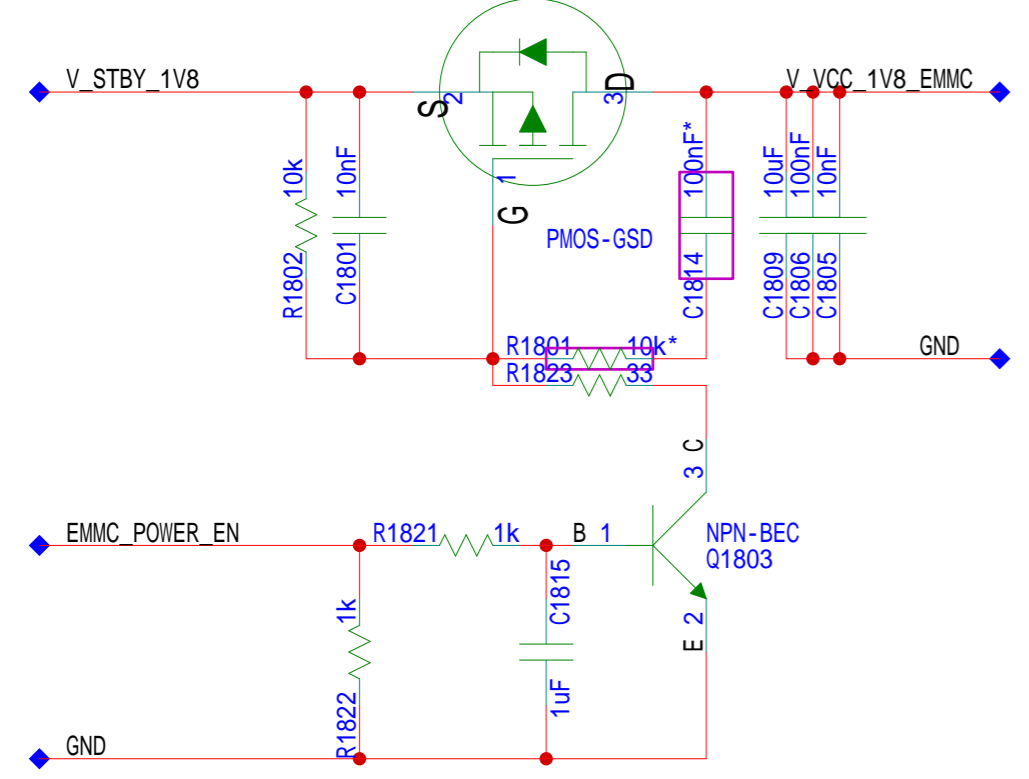
NC/RFU	G3	
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VDDIM/VDDI	C2	C1813	100nF	V_VDDI_EMMC
GND				

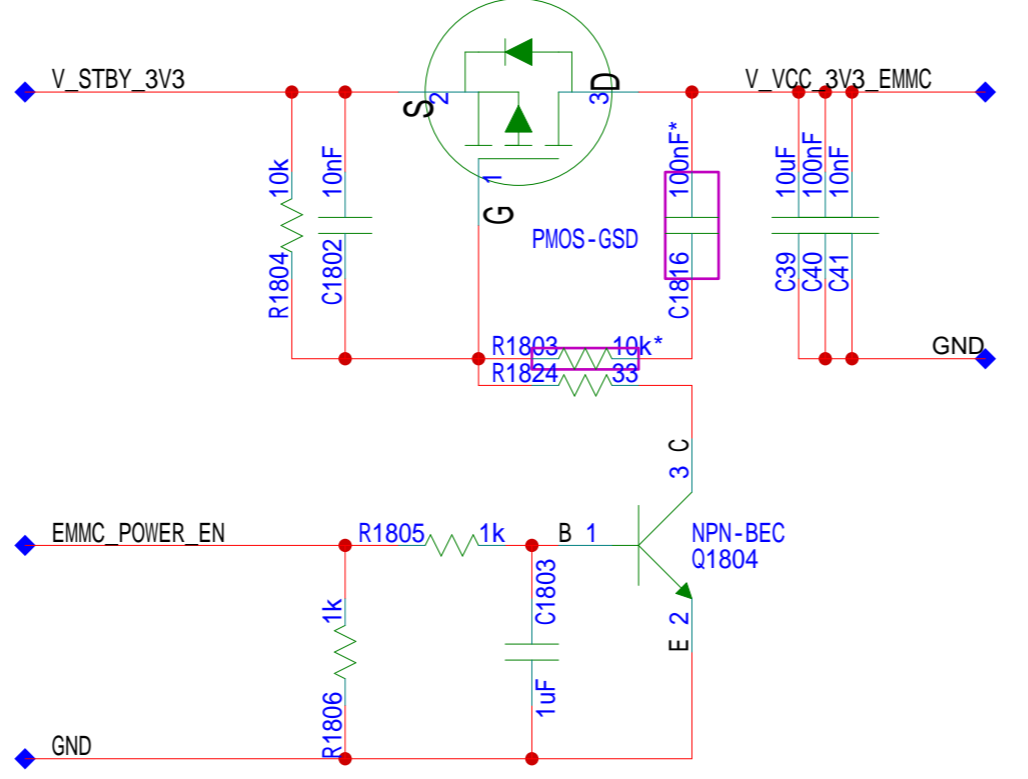
V_VCC_1V8_EMMC	R1816	10k	EMMC_DATA0
	R1817	10k	EMMC_DATA1
	R1818	10k	EMMC_DATA2
	R1819	10k	EMMC_DATA3
	R1815	10k	EMMC_DATA4
	R1814	10k	EMMC_DATA5
	R1813	10k	EMMC_DATA6
	R1812	10k	EMMC_DATA7
	R1811	10k	EMMC_CMD
	R1820	20k	EMMC_DS
	R1833	10k	EMMC_CLK
			GND
			GND

Follow DEMO EMMC_CLK must PD with 10K

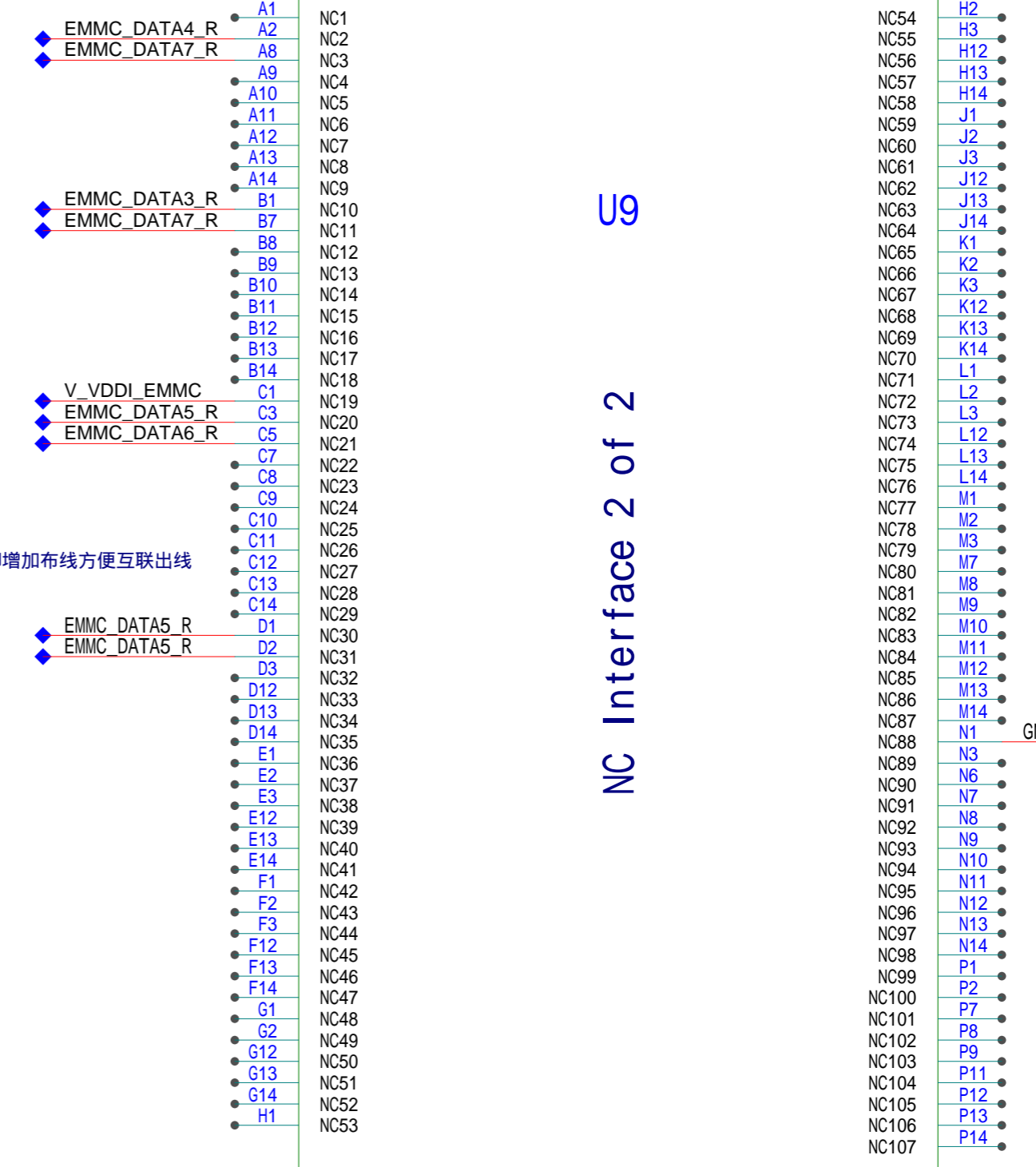
Q1801



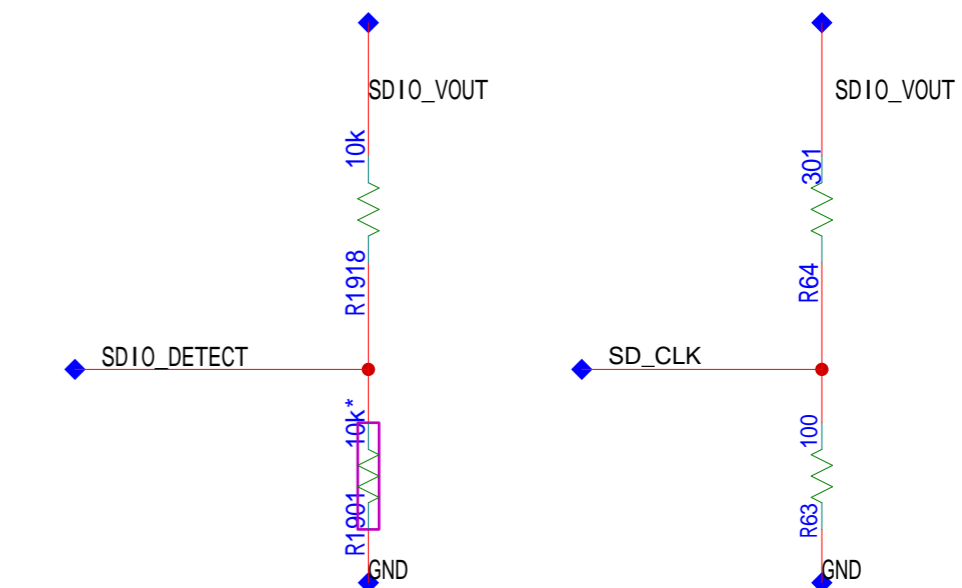
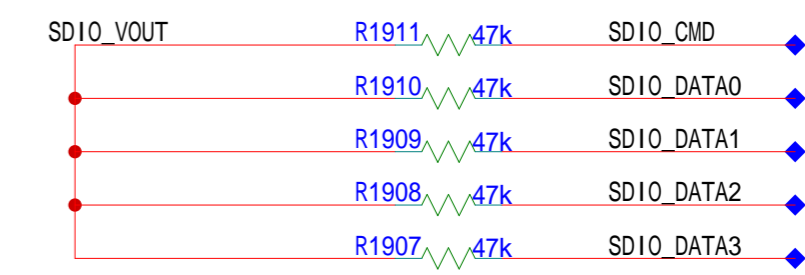
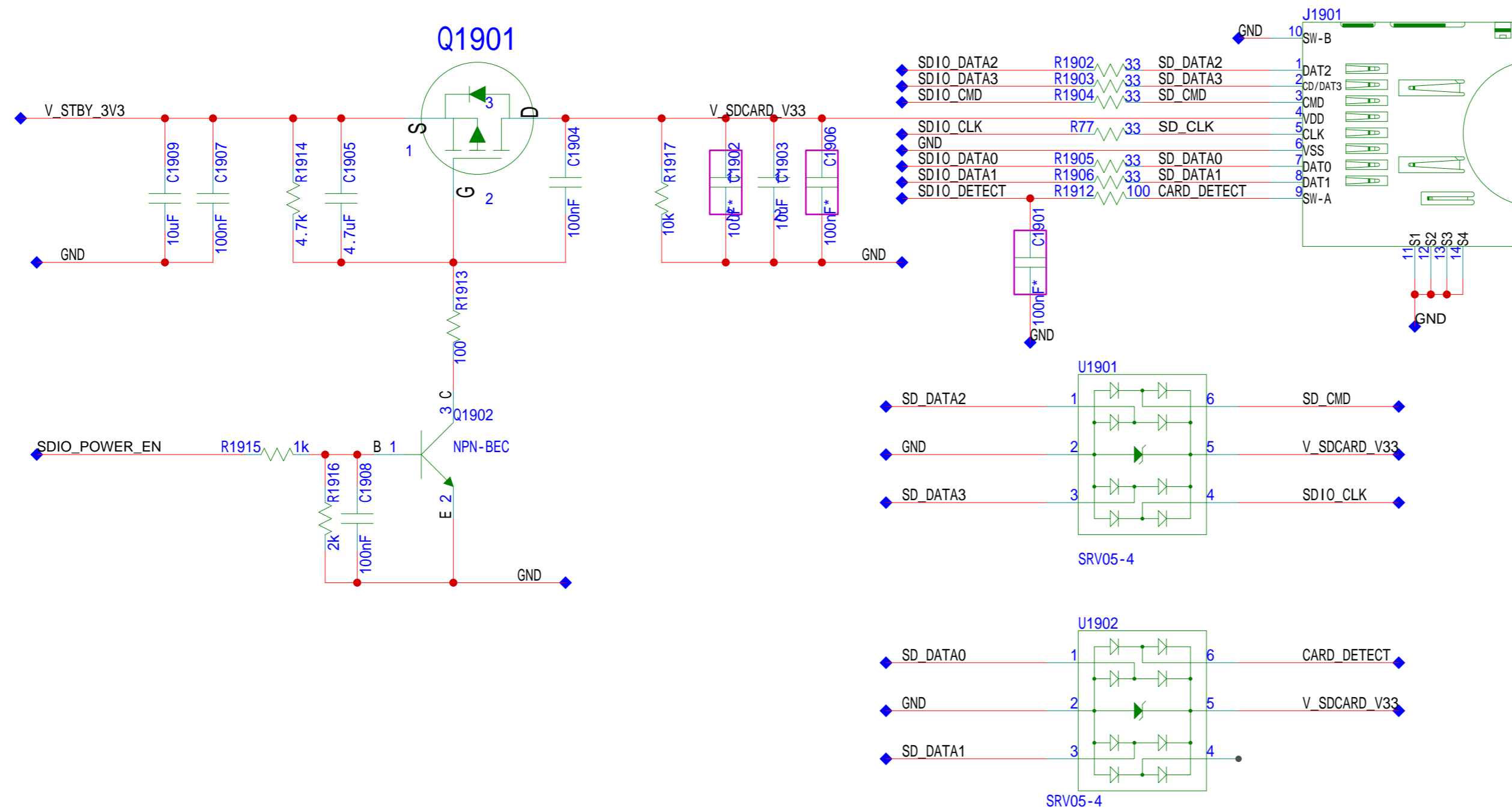
Q1802



NC管脚增加布线方便互联出线

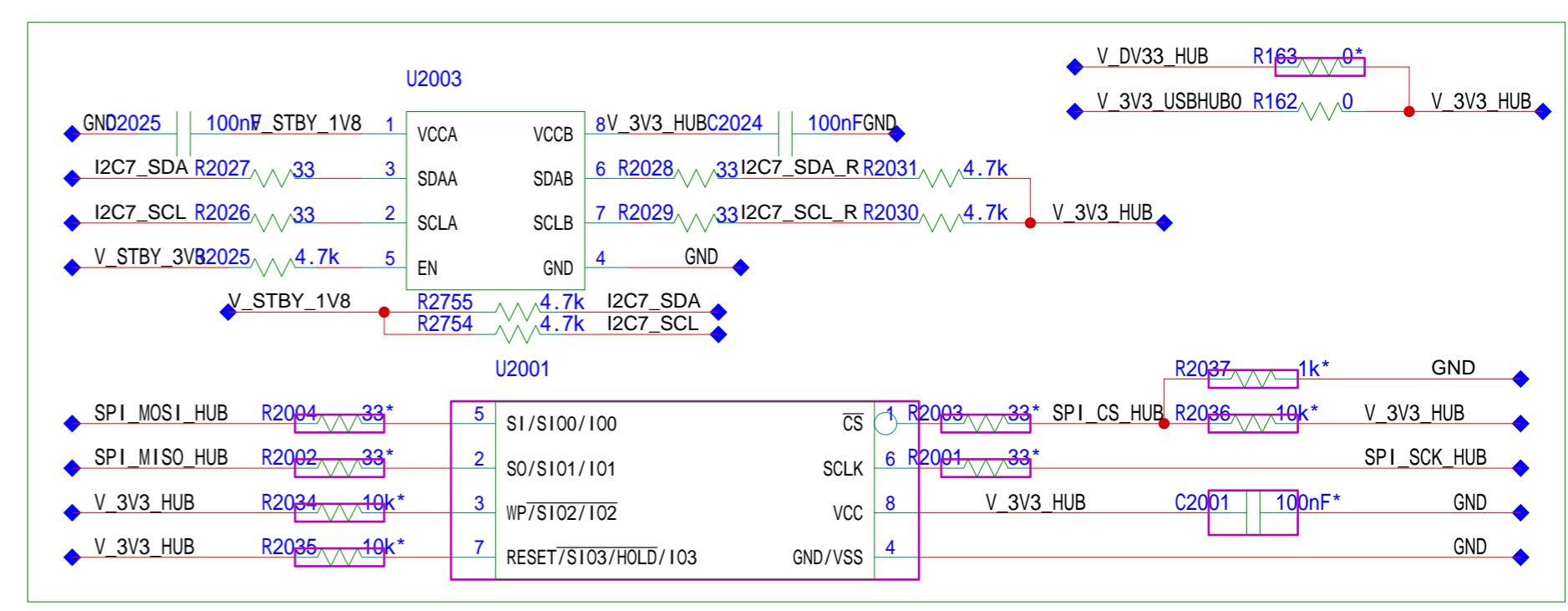
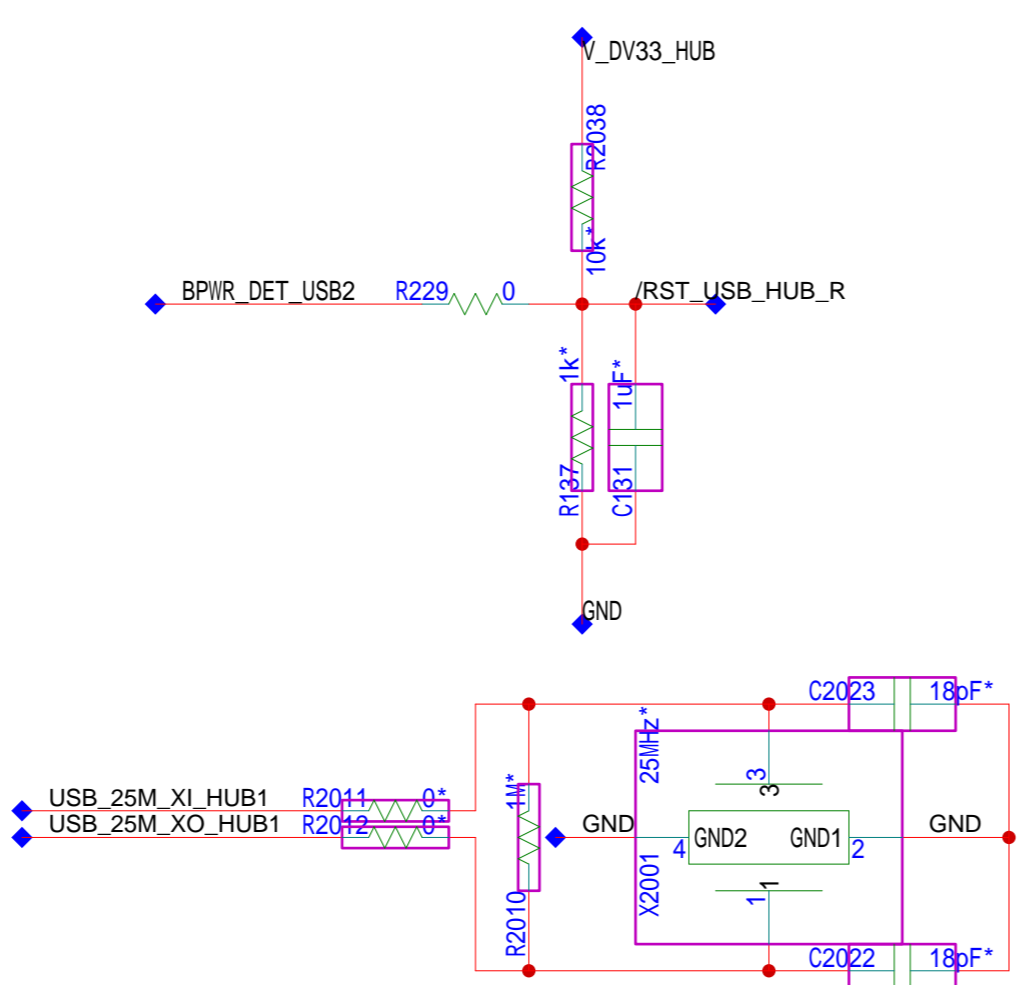
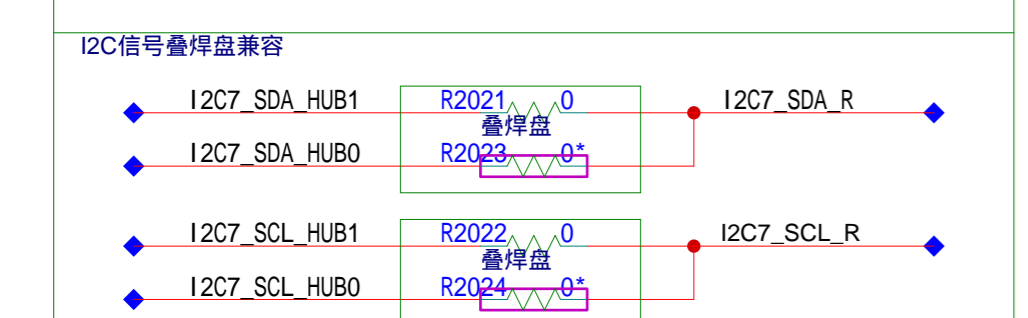
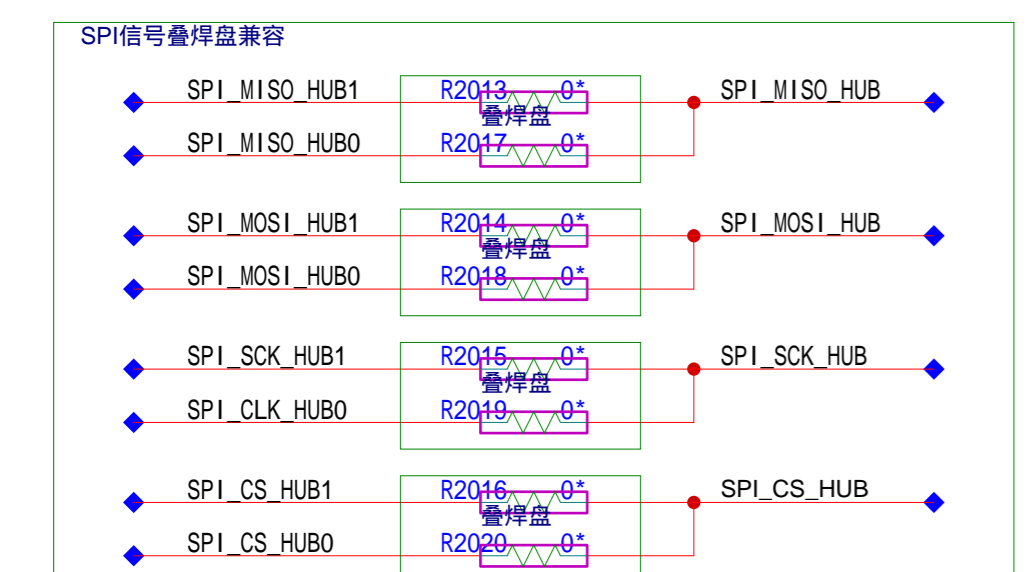
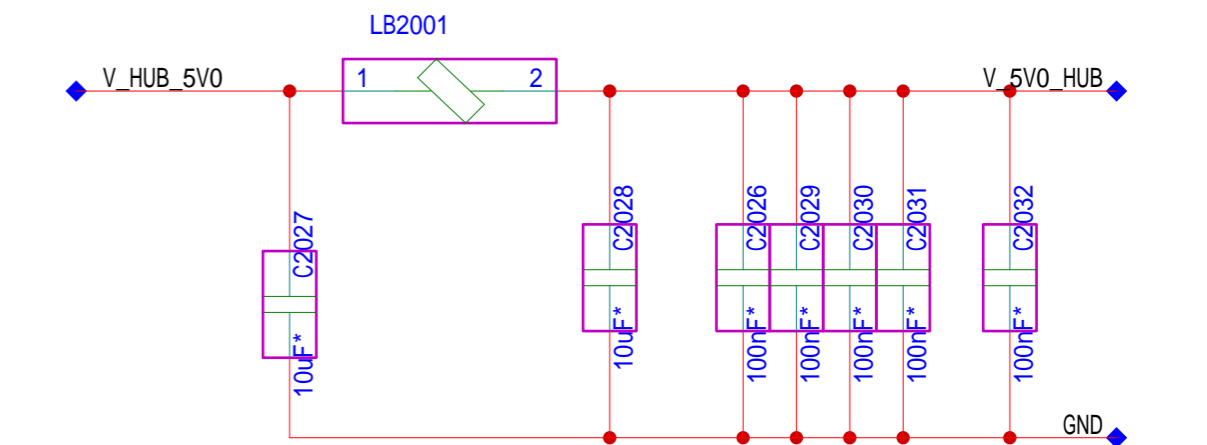
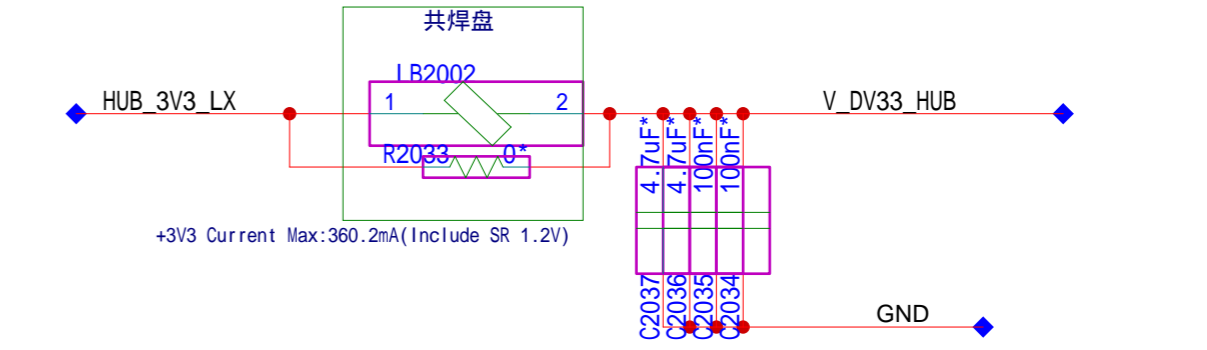
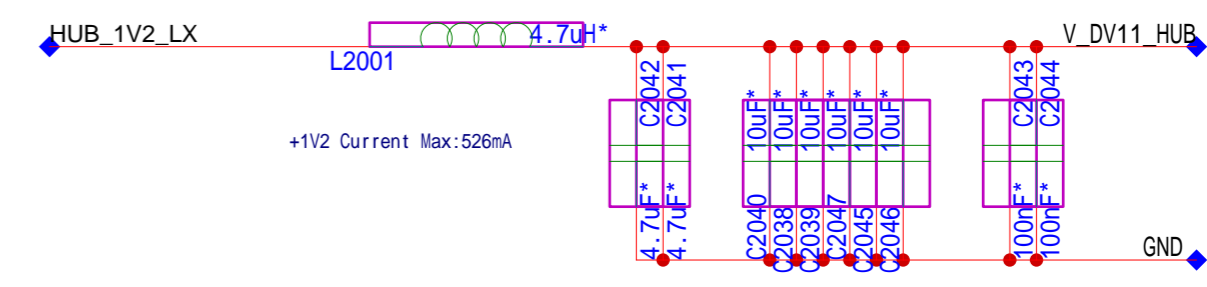
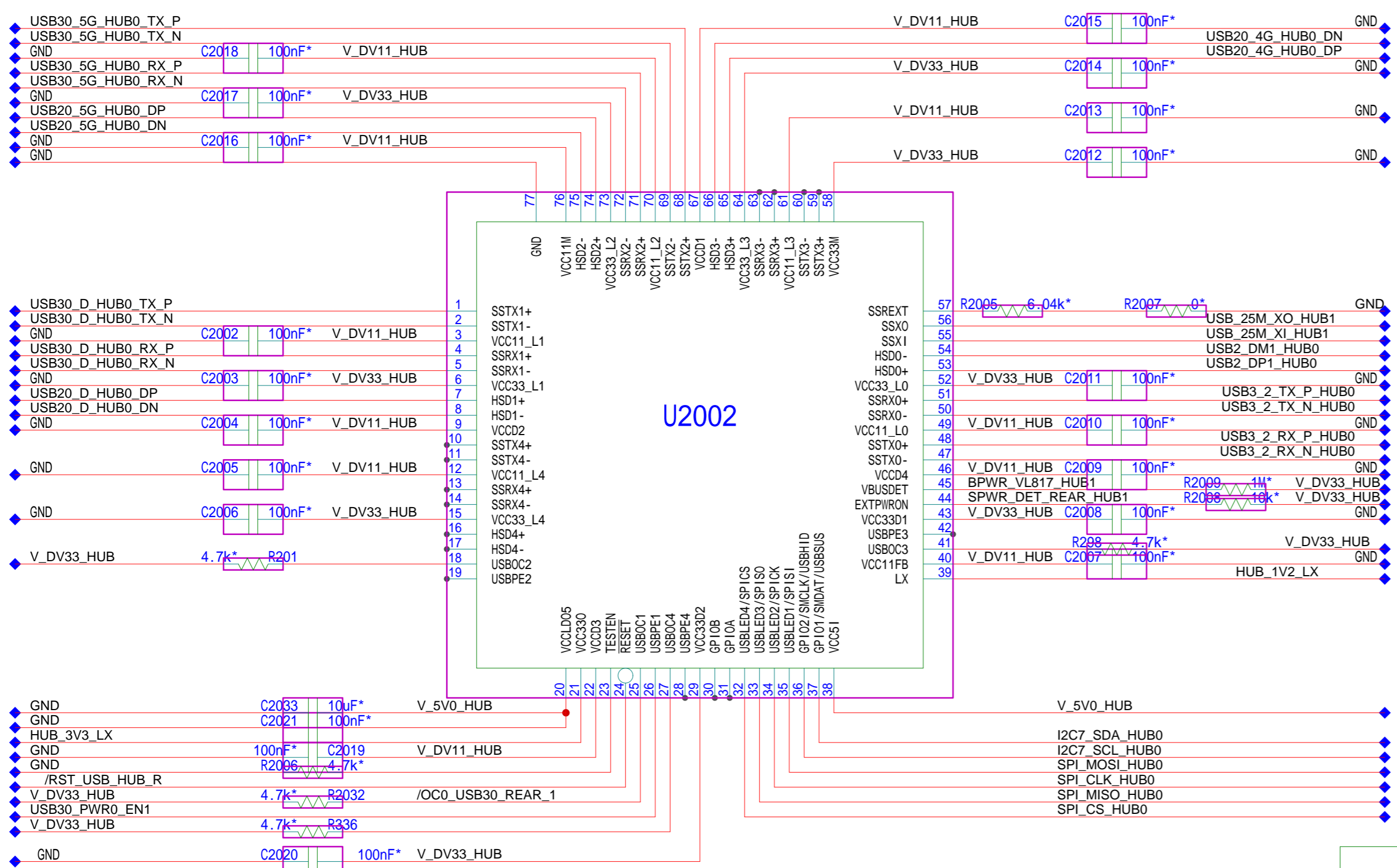


NC Interface 2 of 2



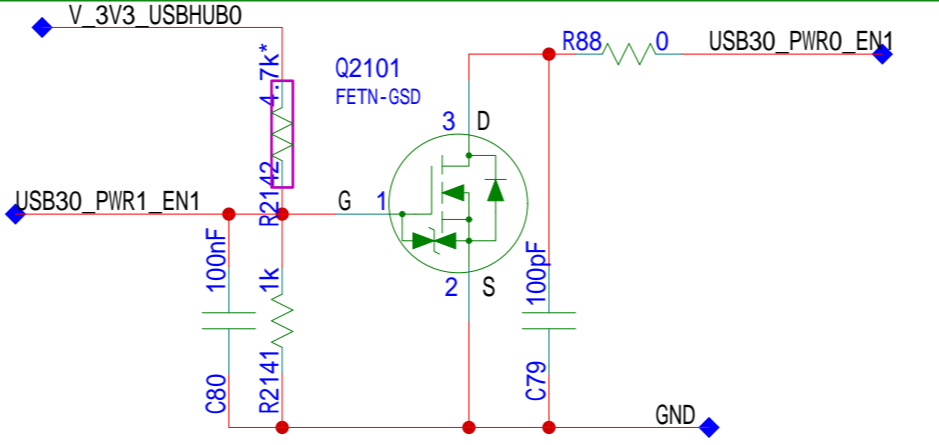
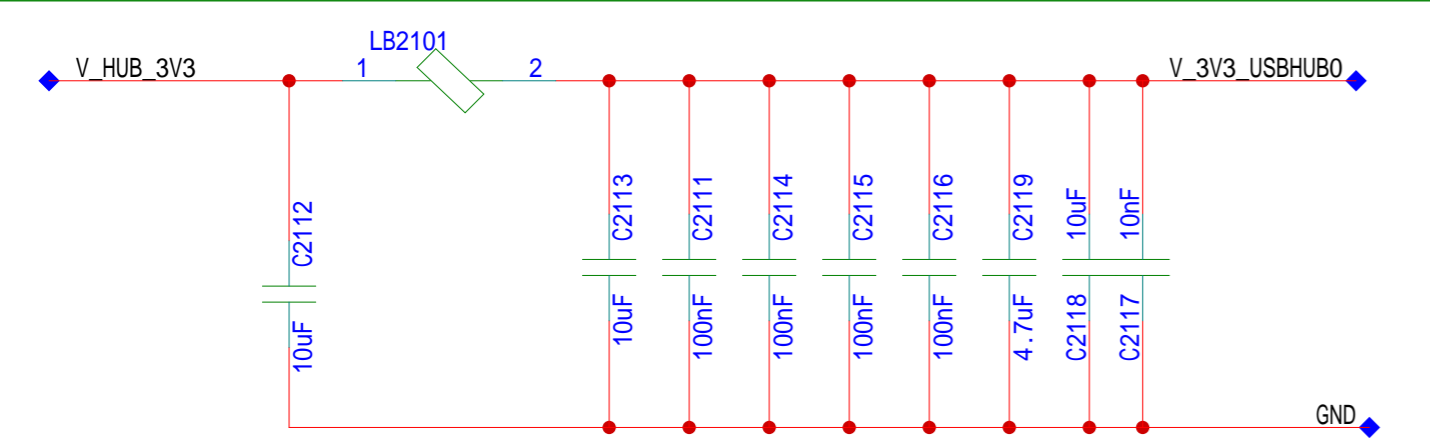
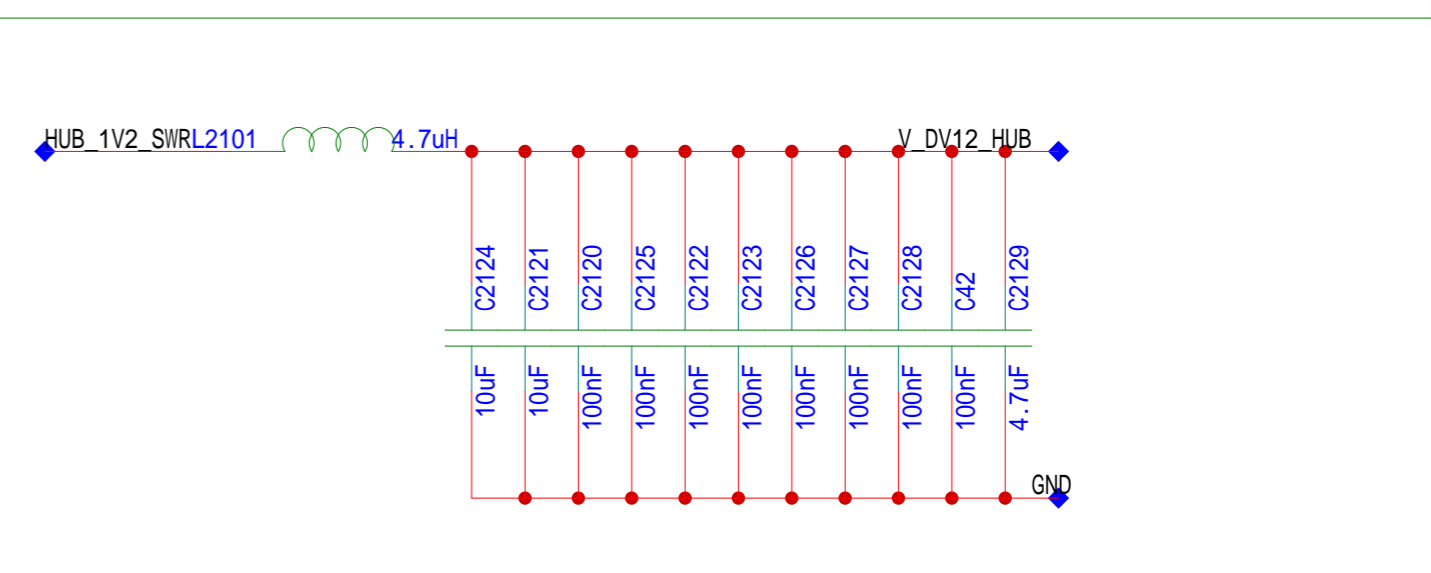
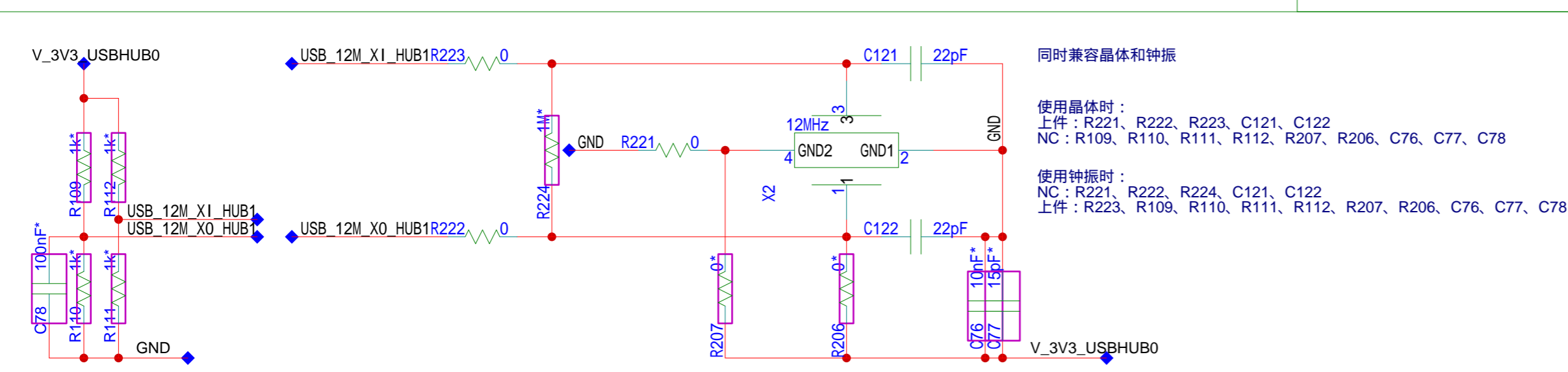
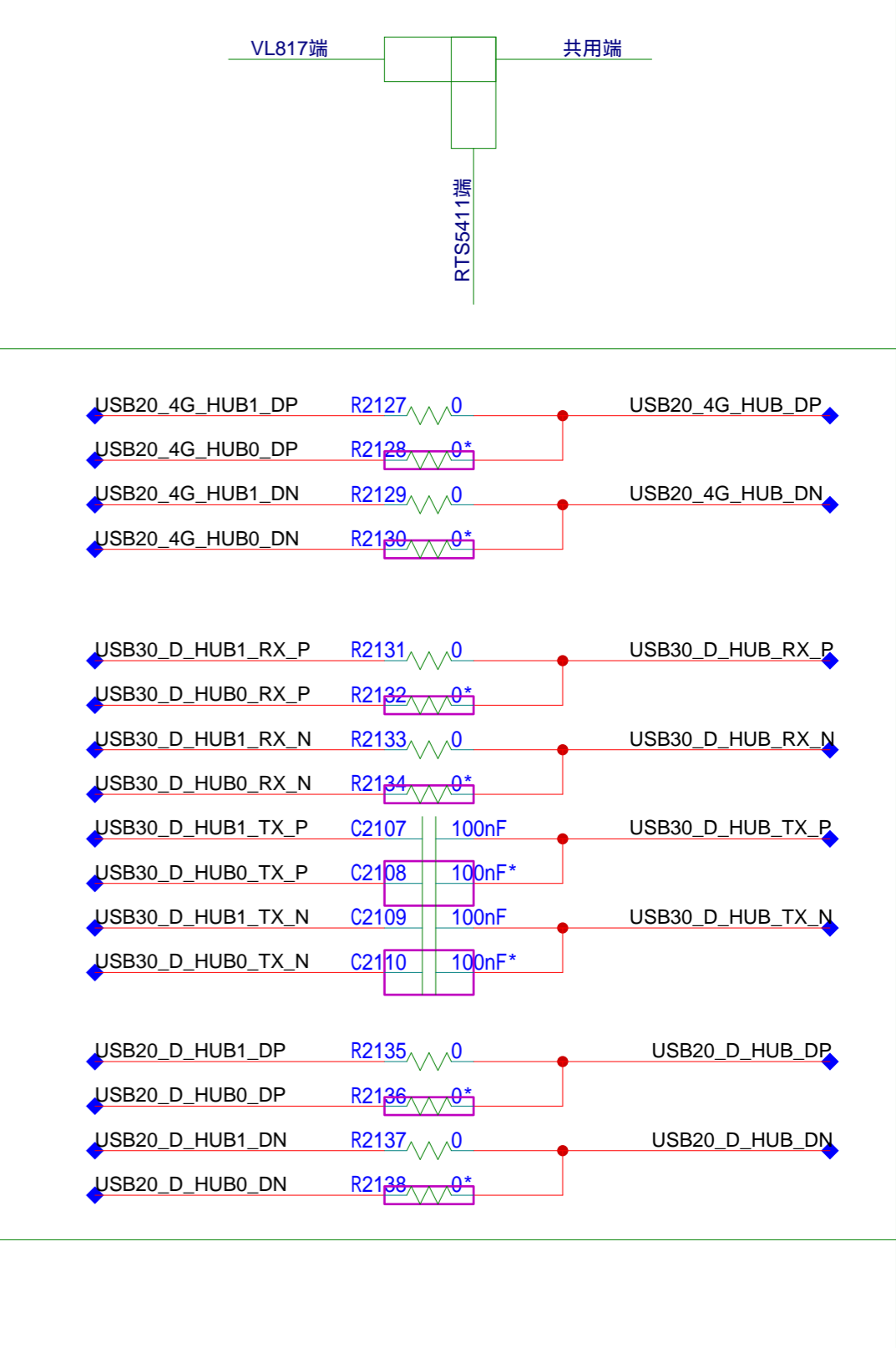
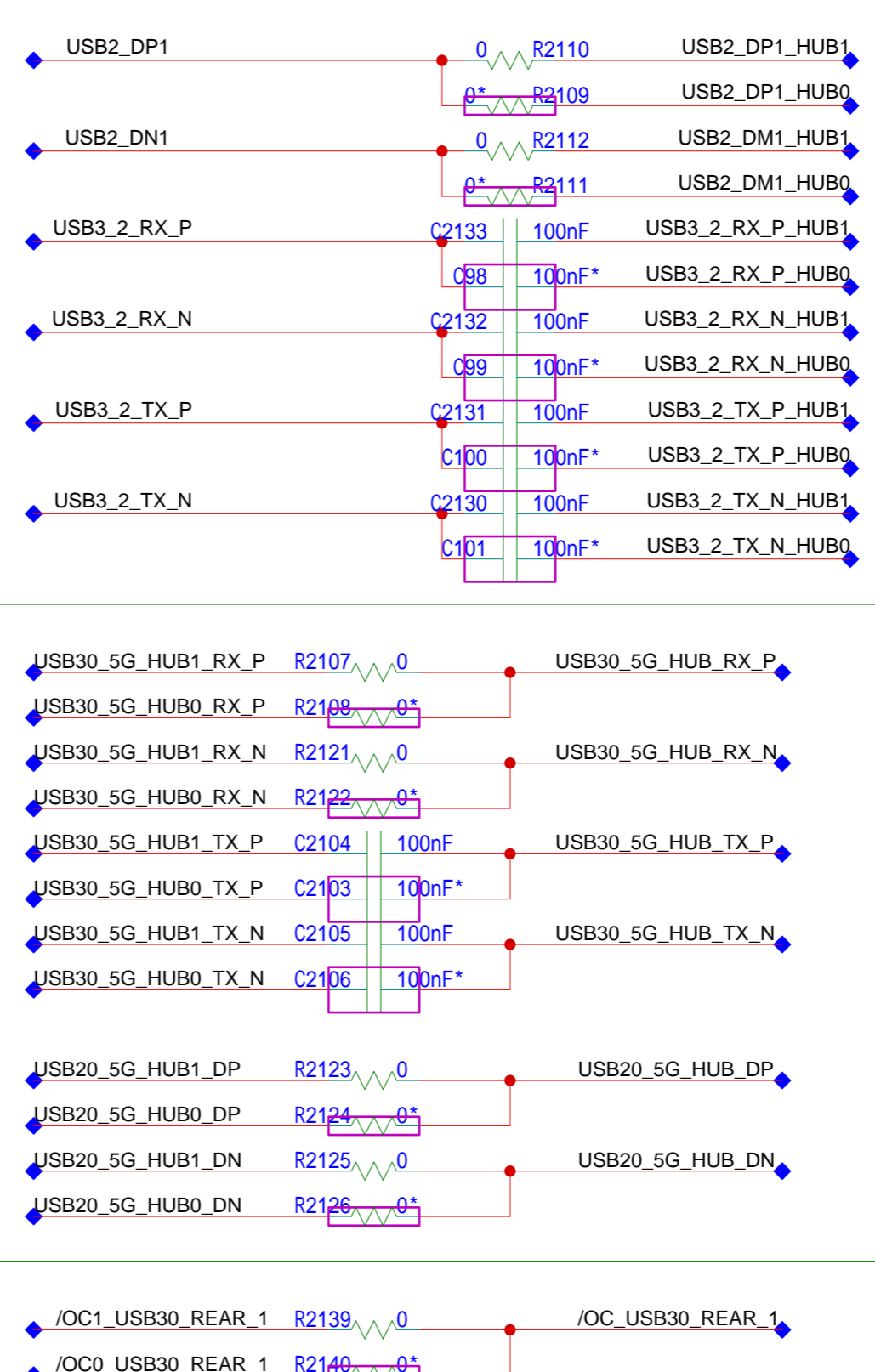
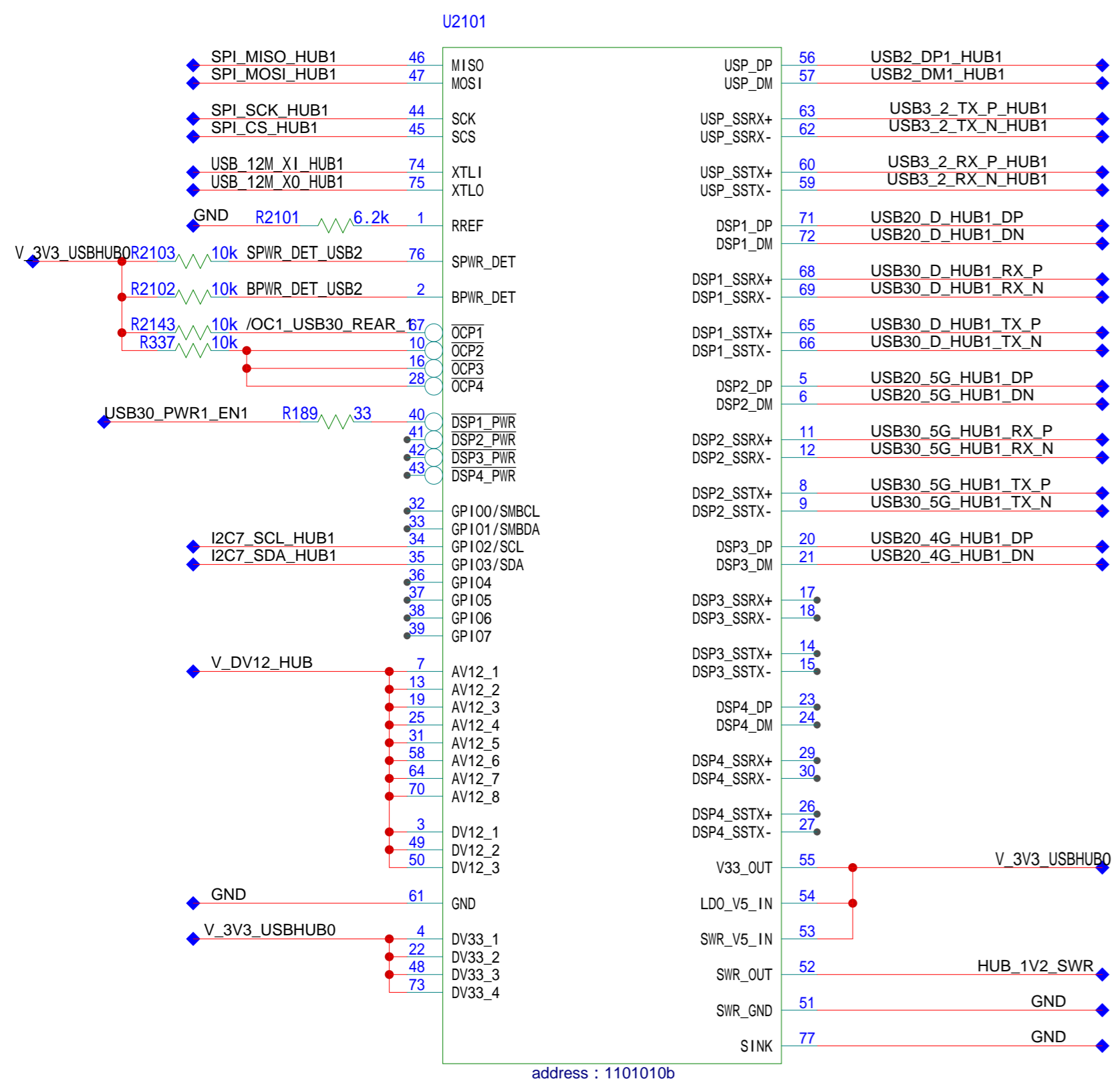
SDIO_DETECT和SD_CLK一定要按这个方案设计

USB3.0 & USB2.0 HUB (兼容设计, 此方案不上件)



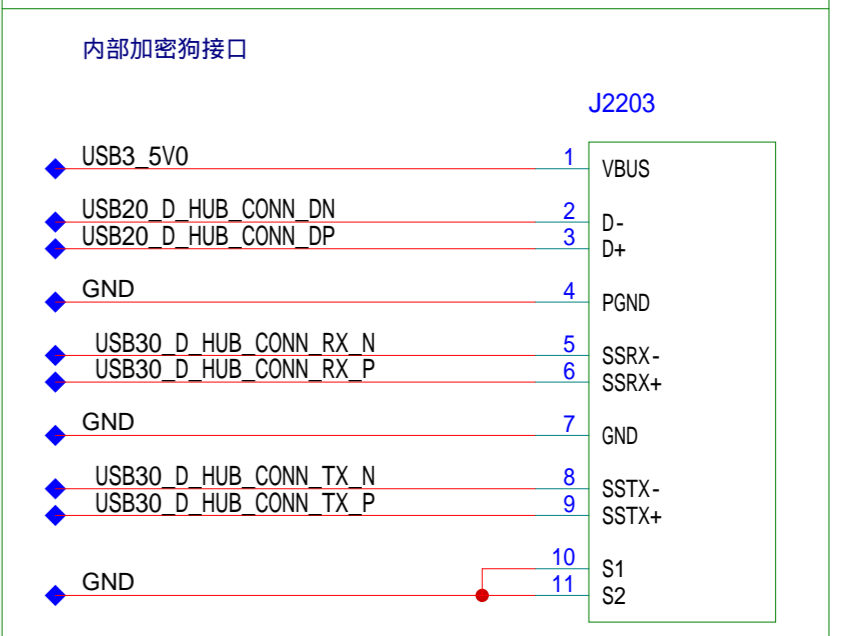
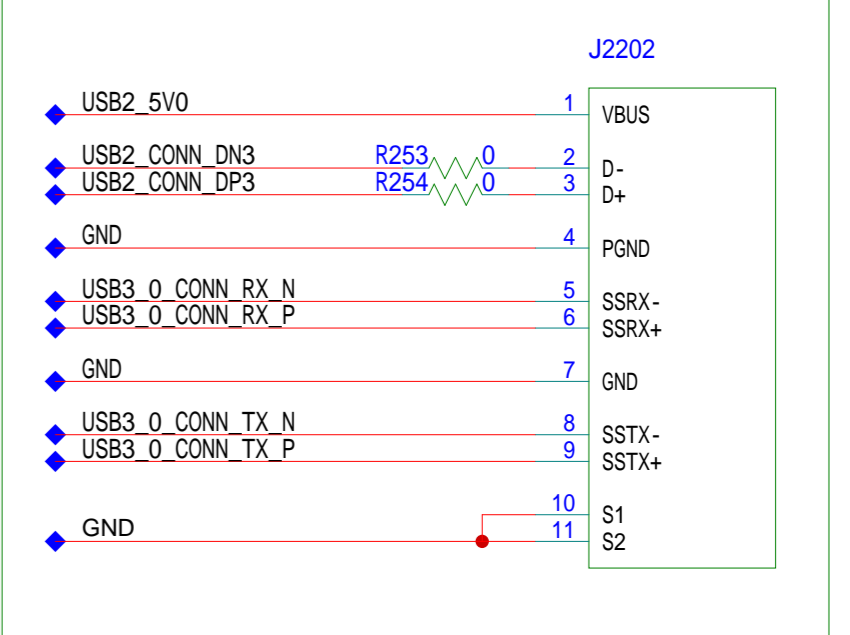
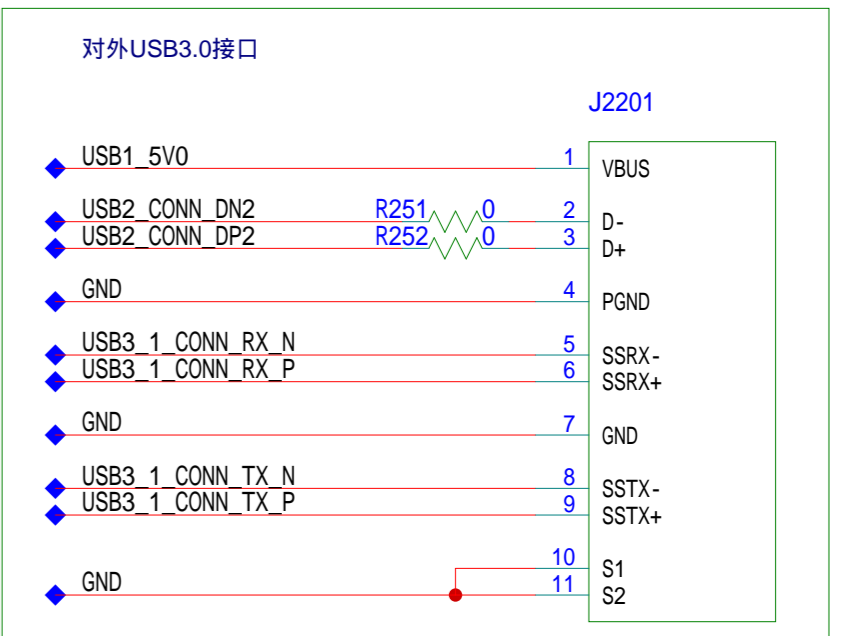
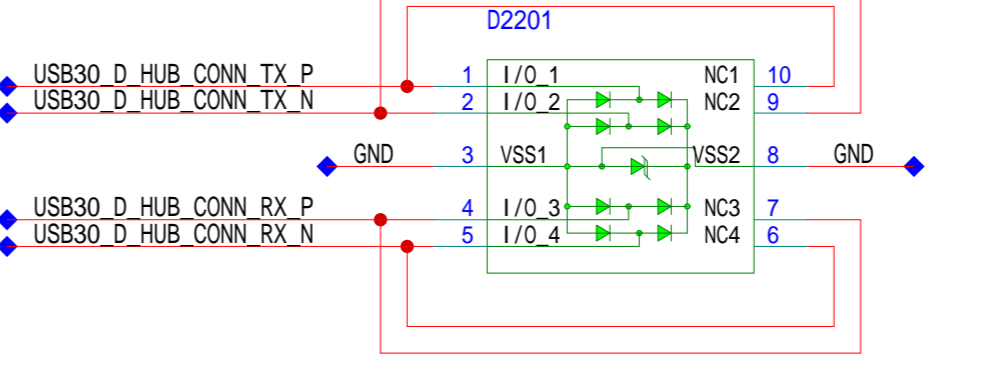
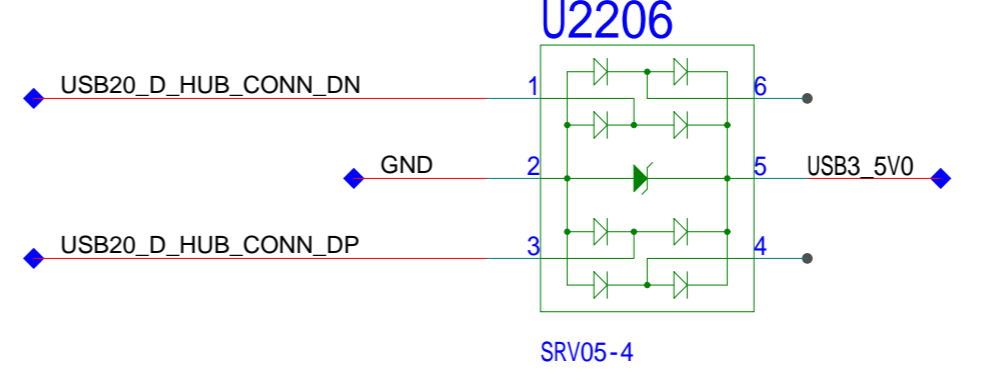
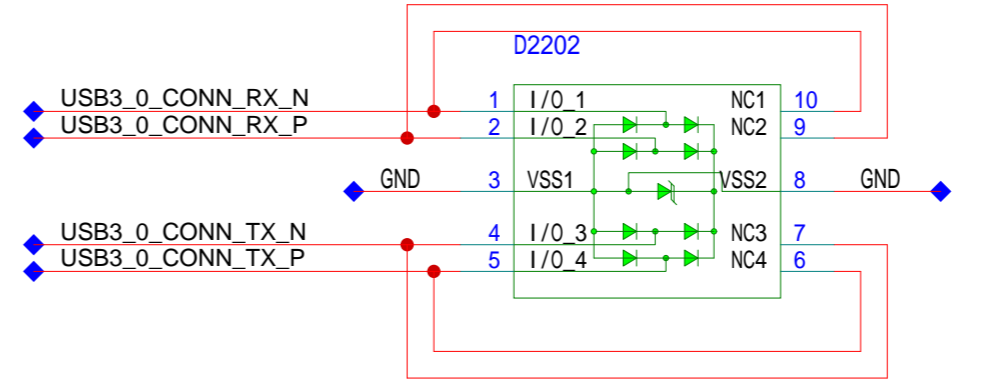
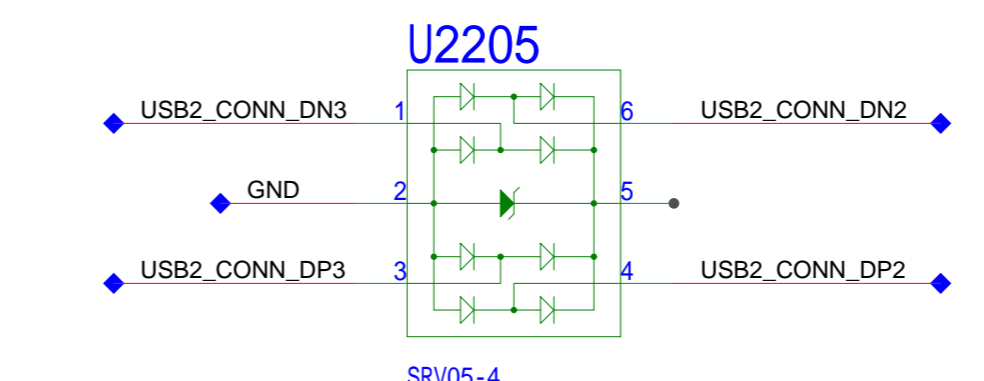
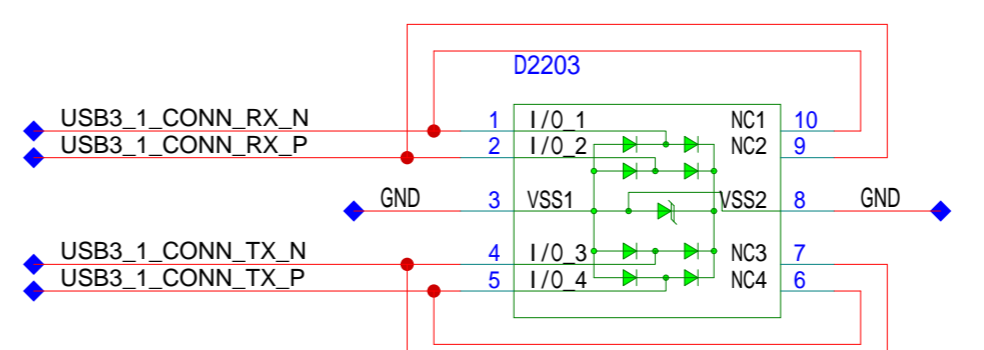
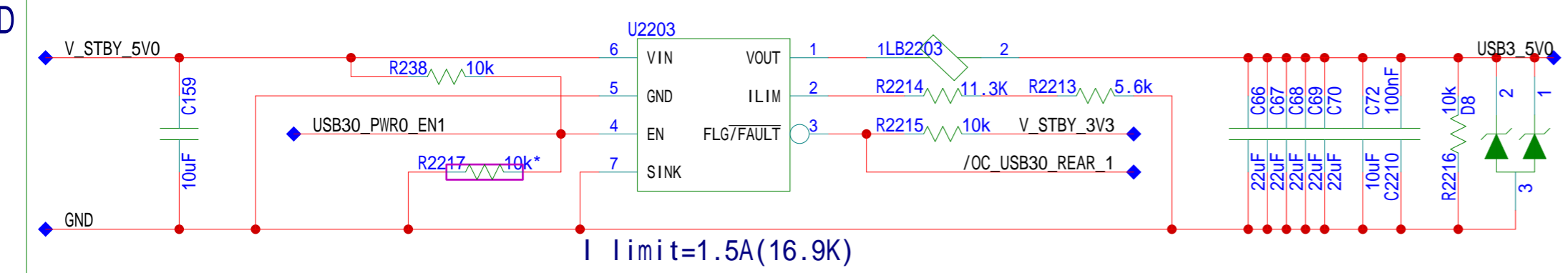
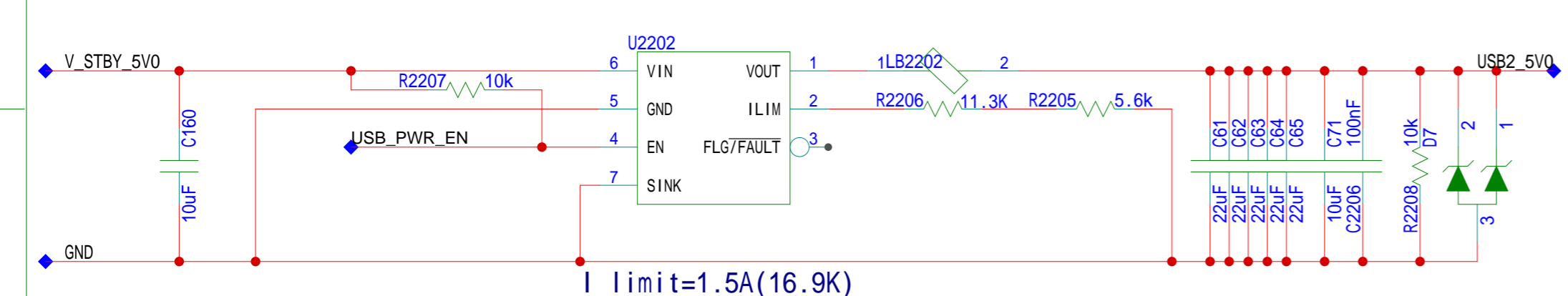
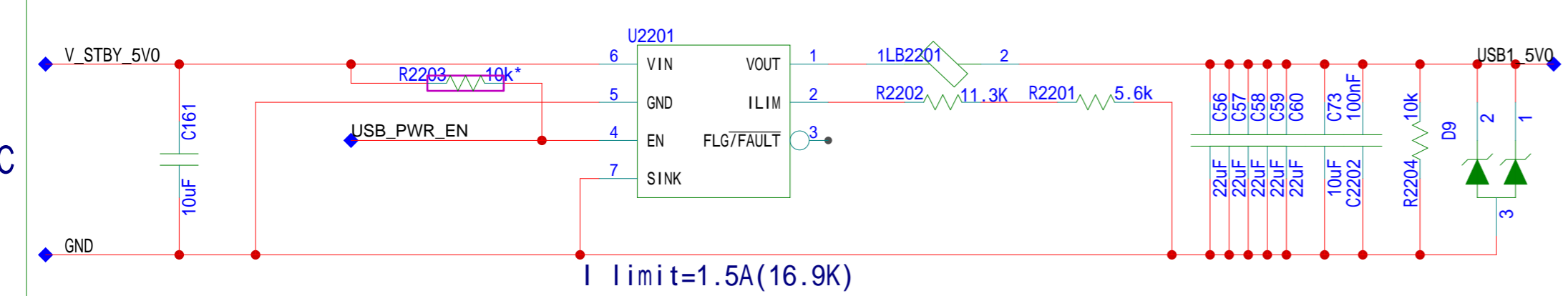
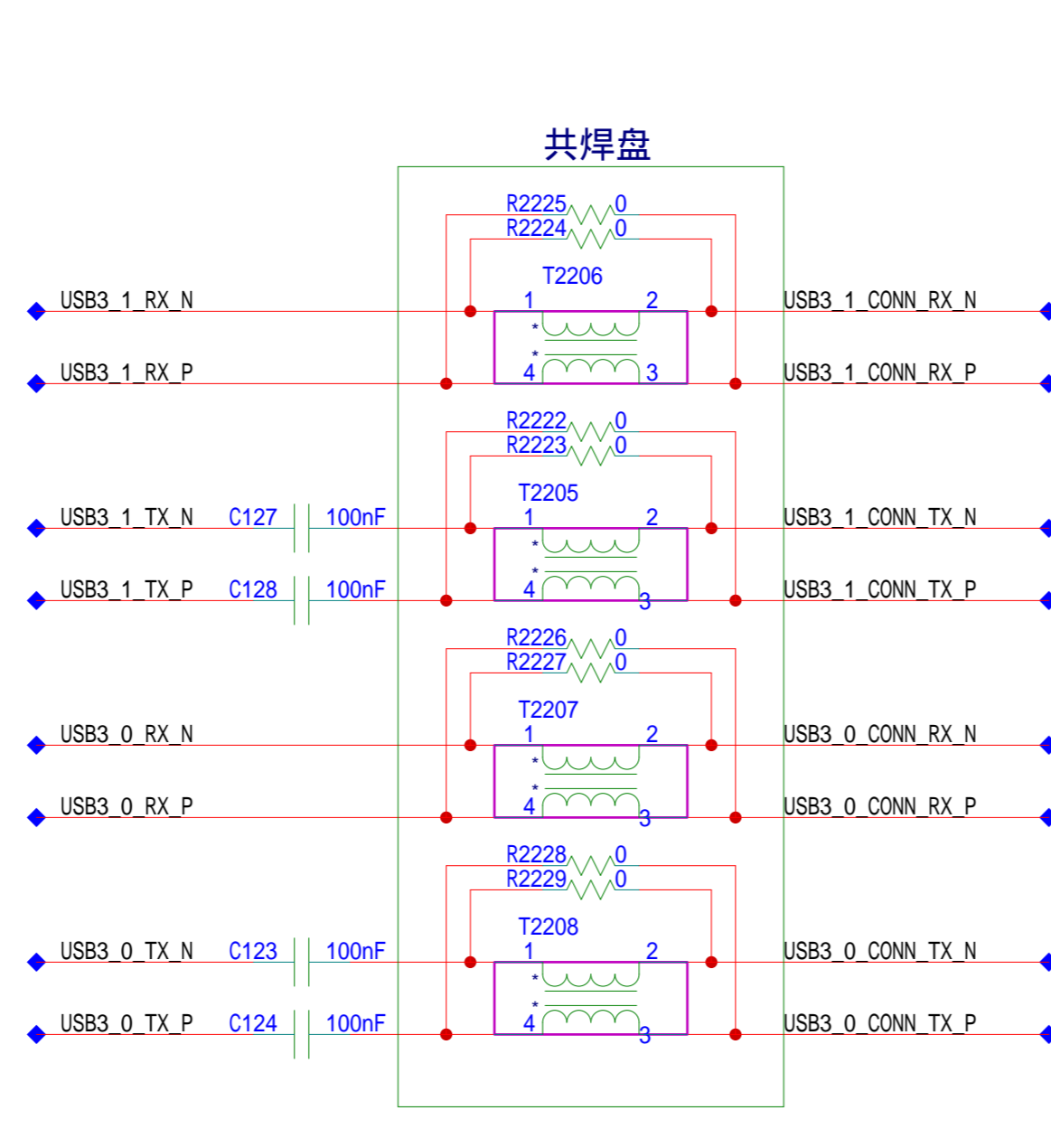
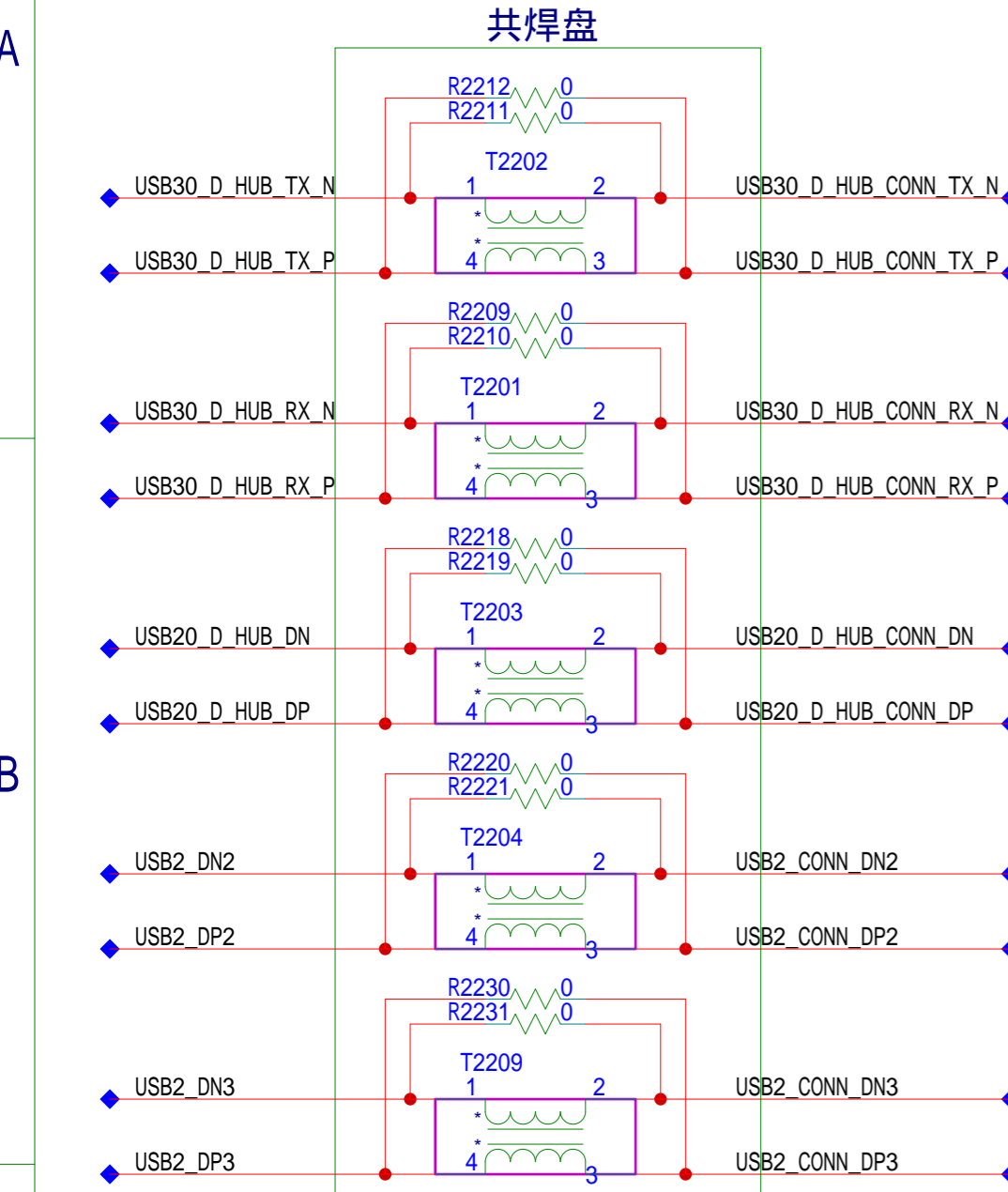
USB3.0 & USB2.0 HUB CHOSE

USB HUB方案兼容，做分叉叠焊盘设计

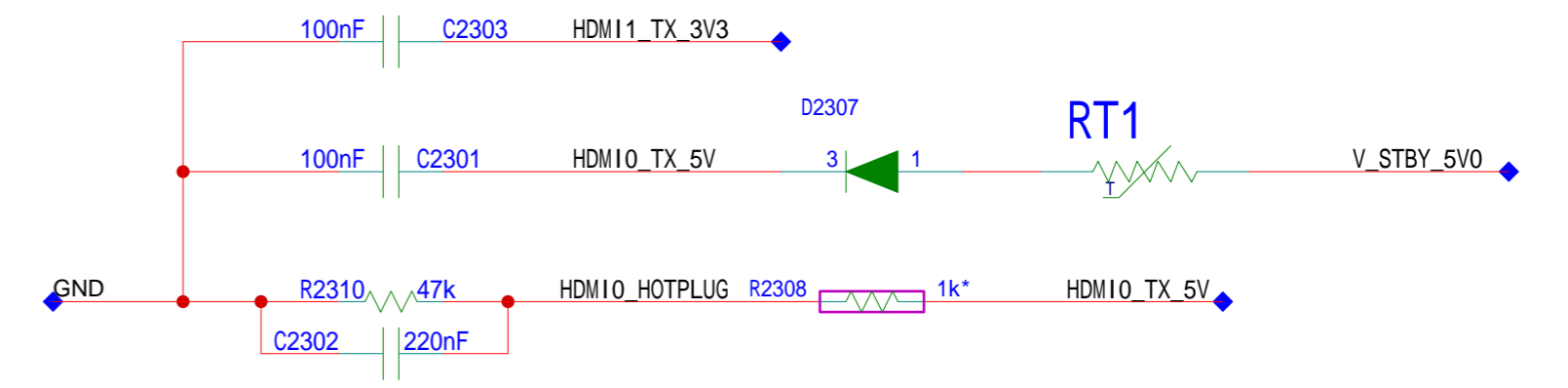
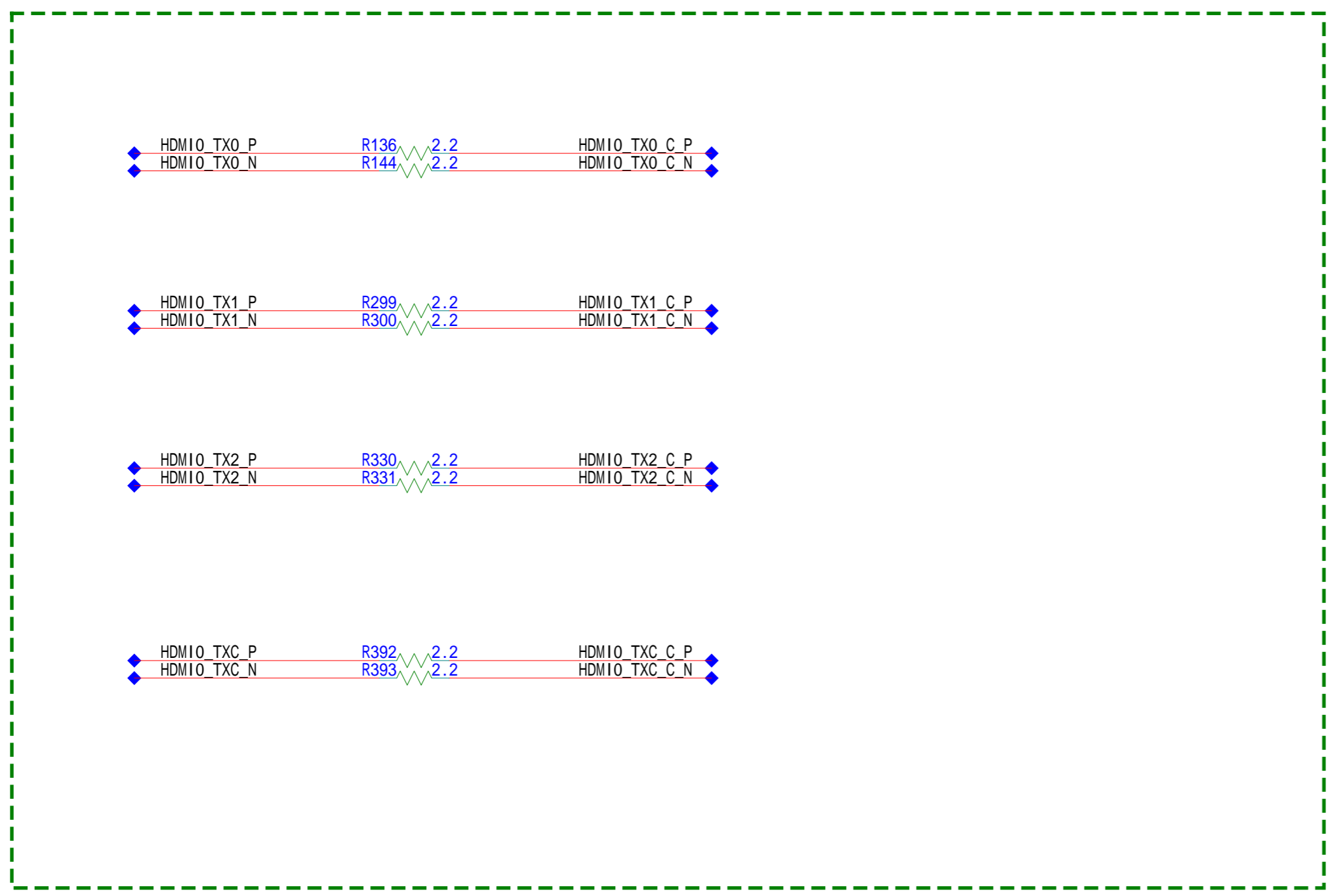
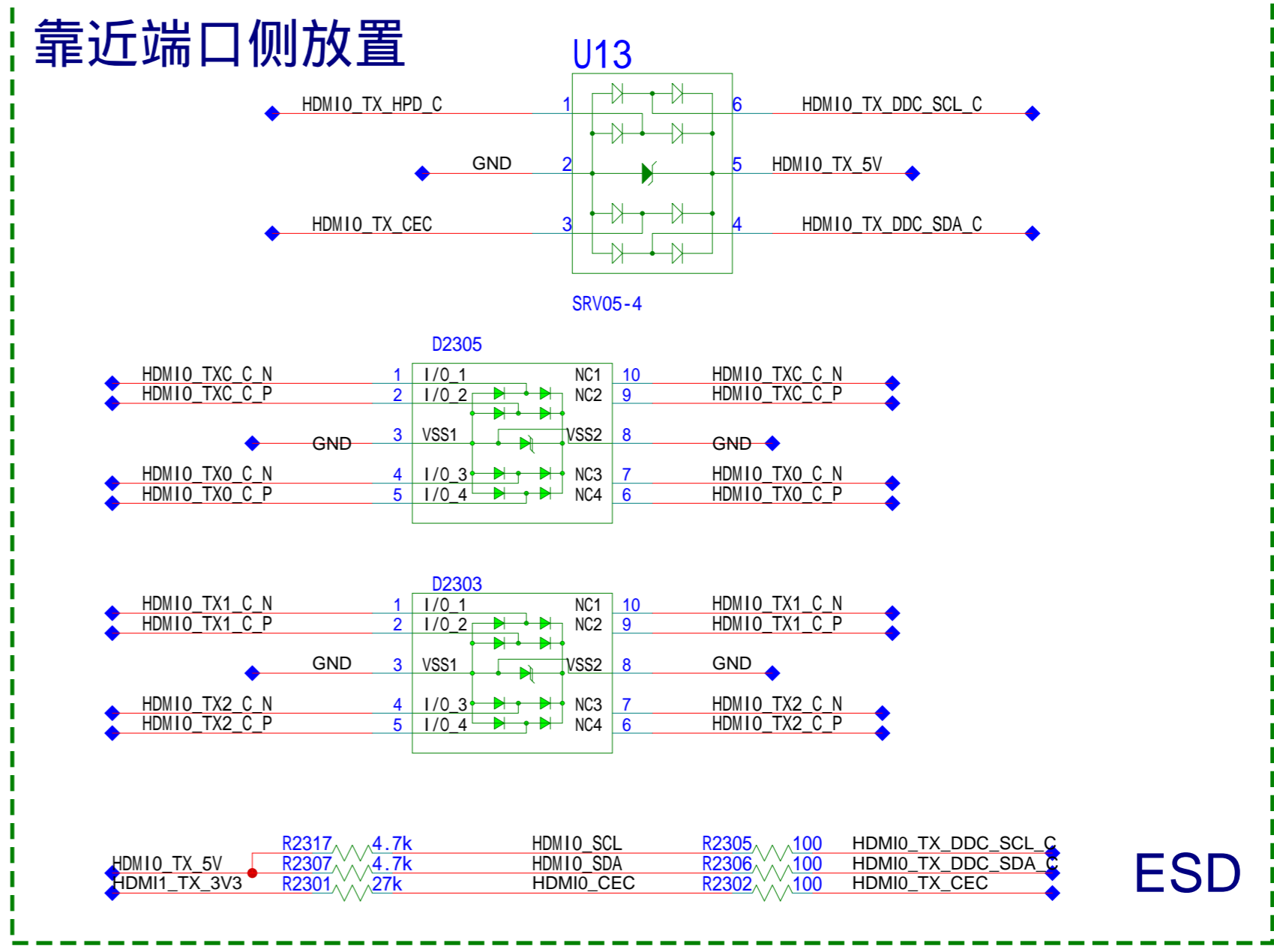
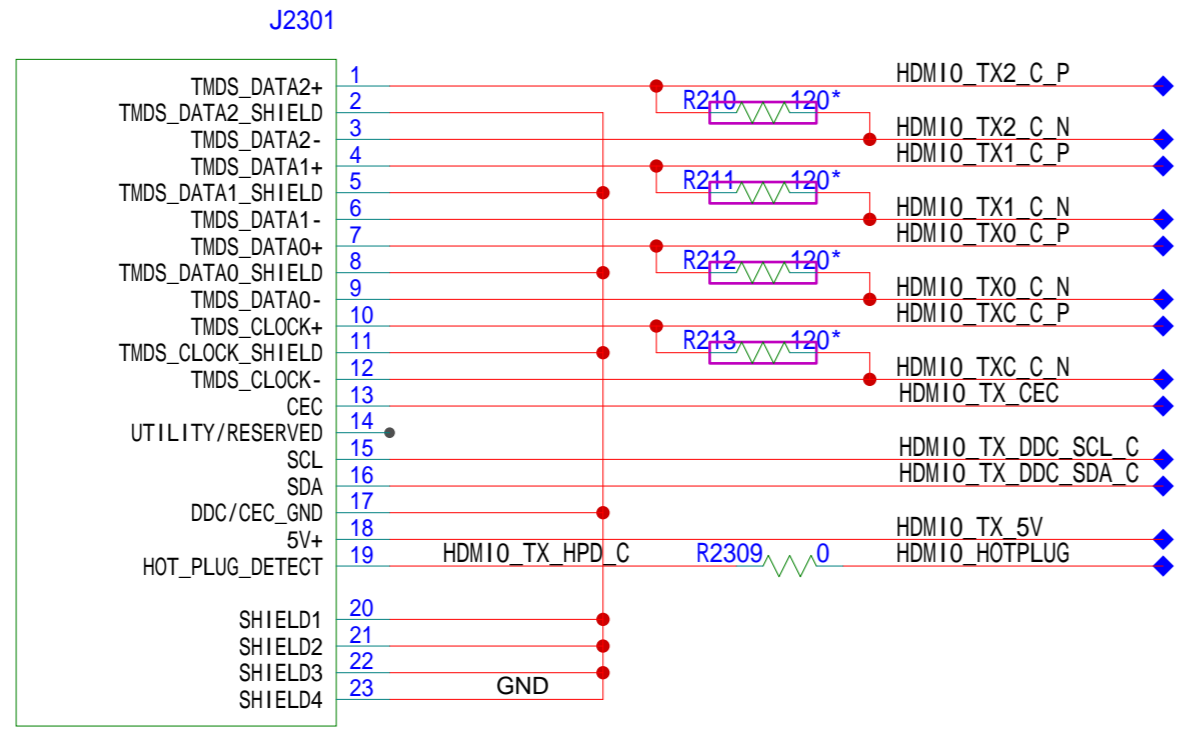


两种HUB的PWR控制逻辑相反，需要兼容两种高低电平逻辑进行设计；

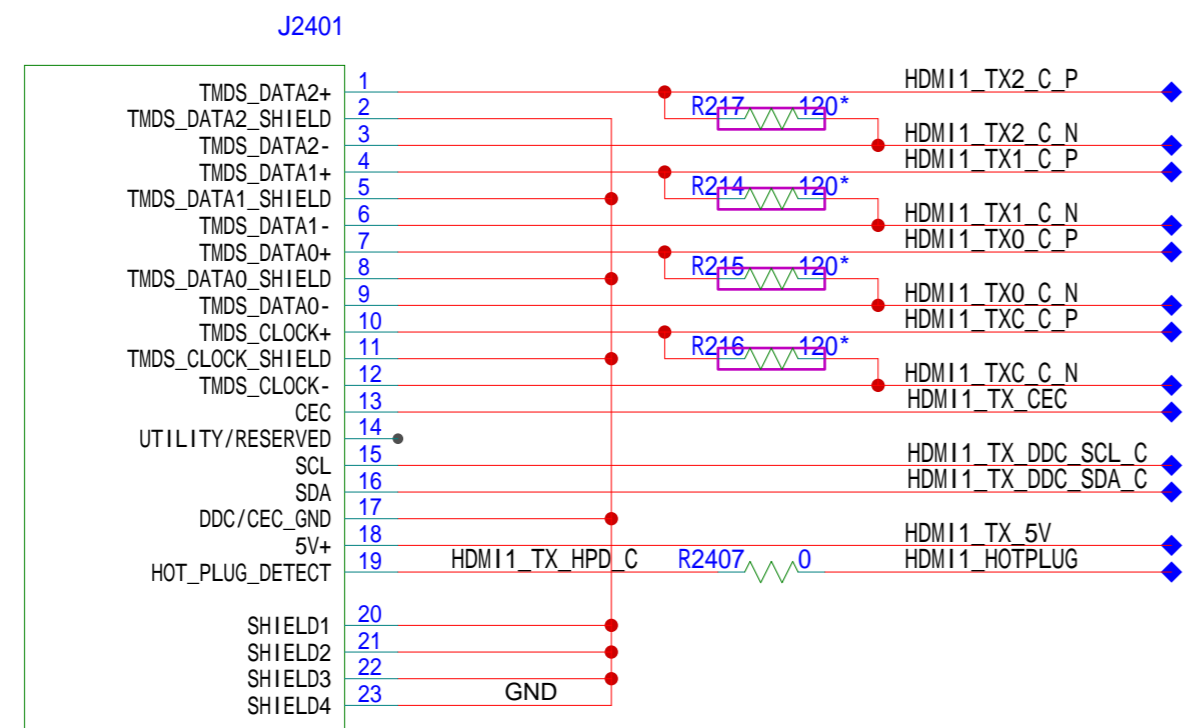
USB3.0 + USB2.0 Connector + Dongle(Type-A)



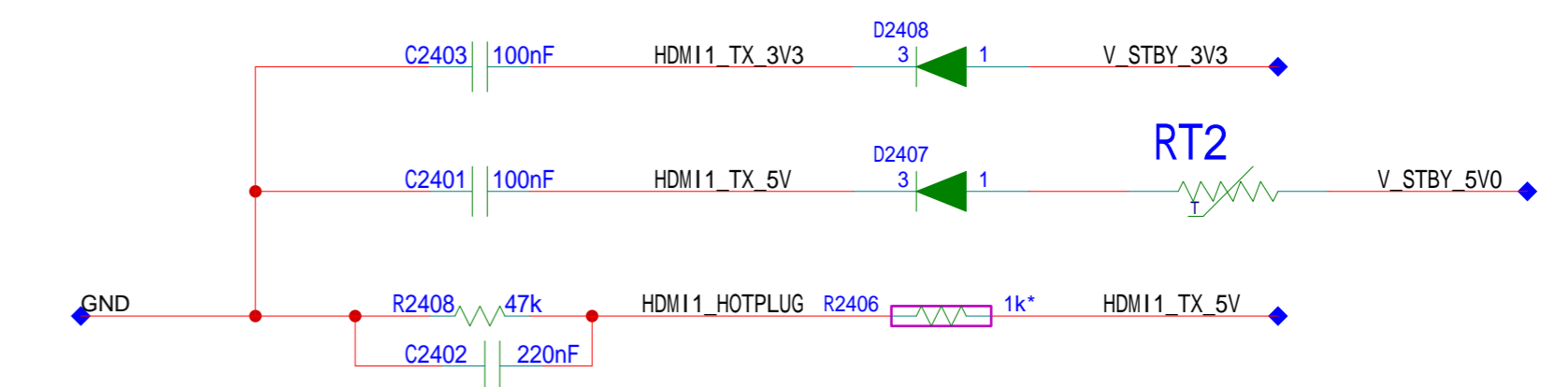
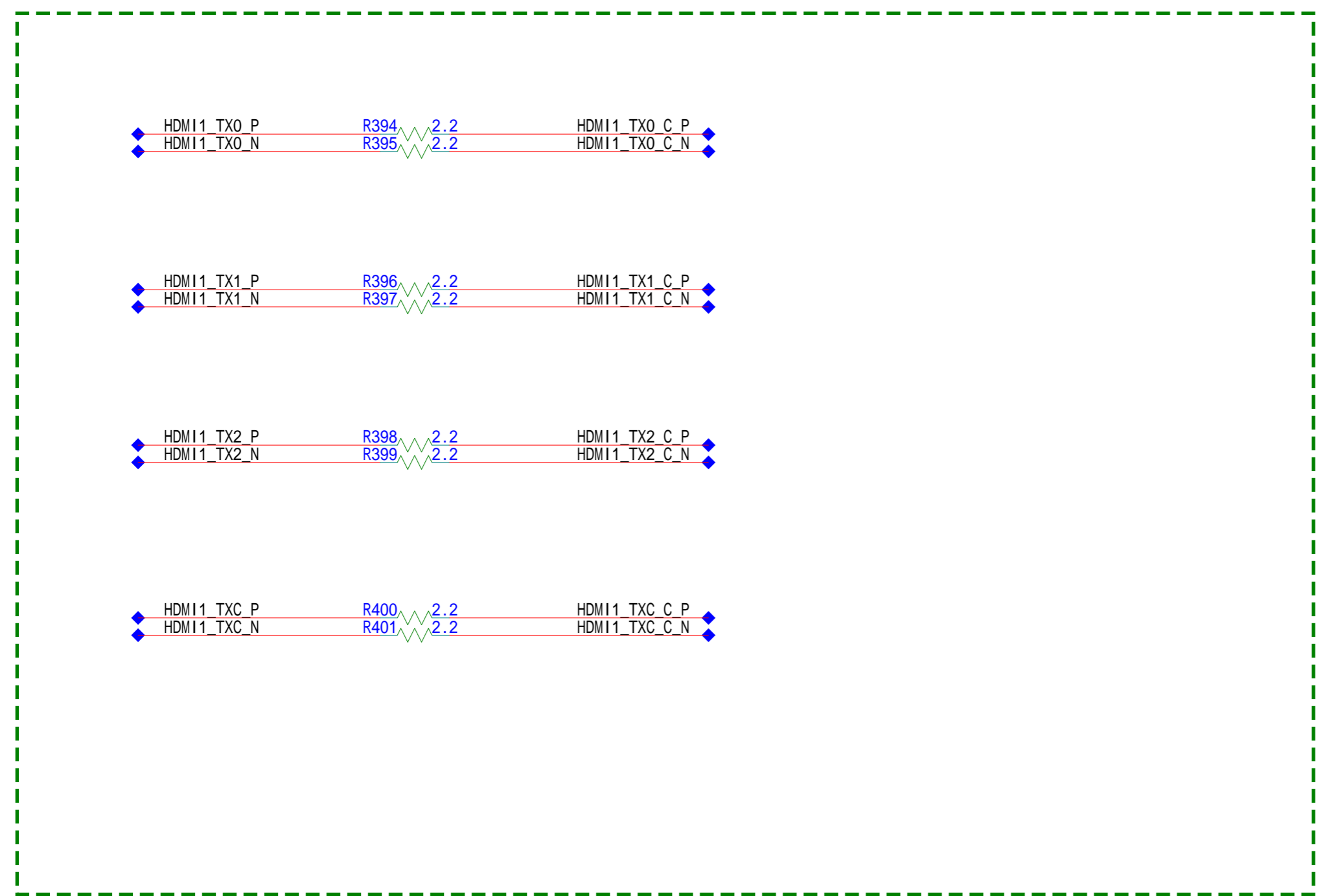
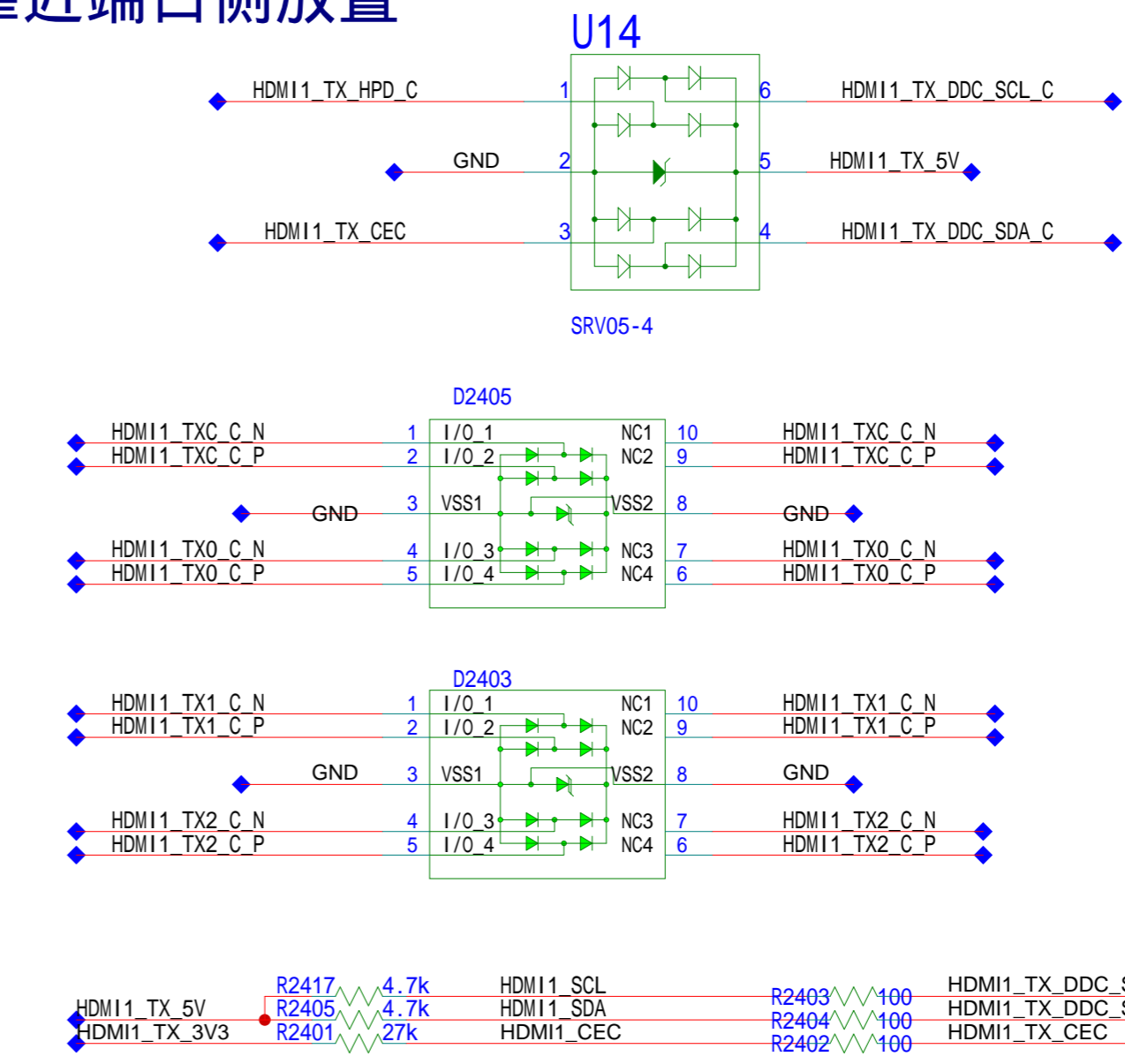
HDMI 2.0 OUT



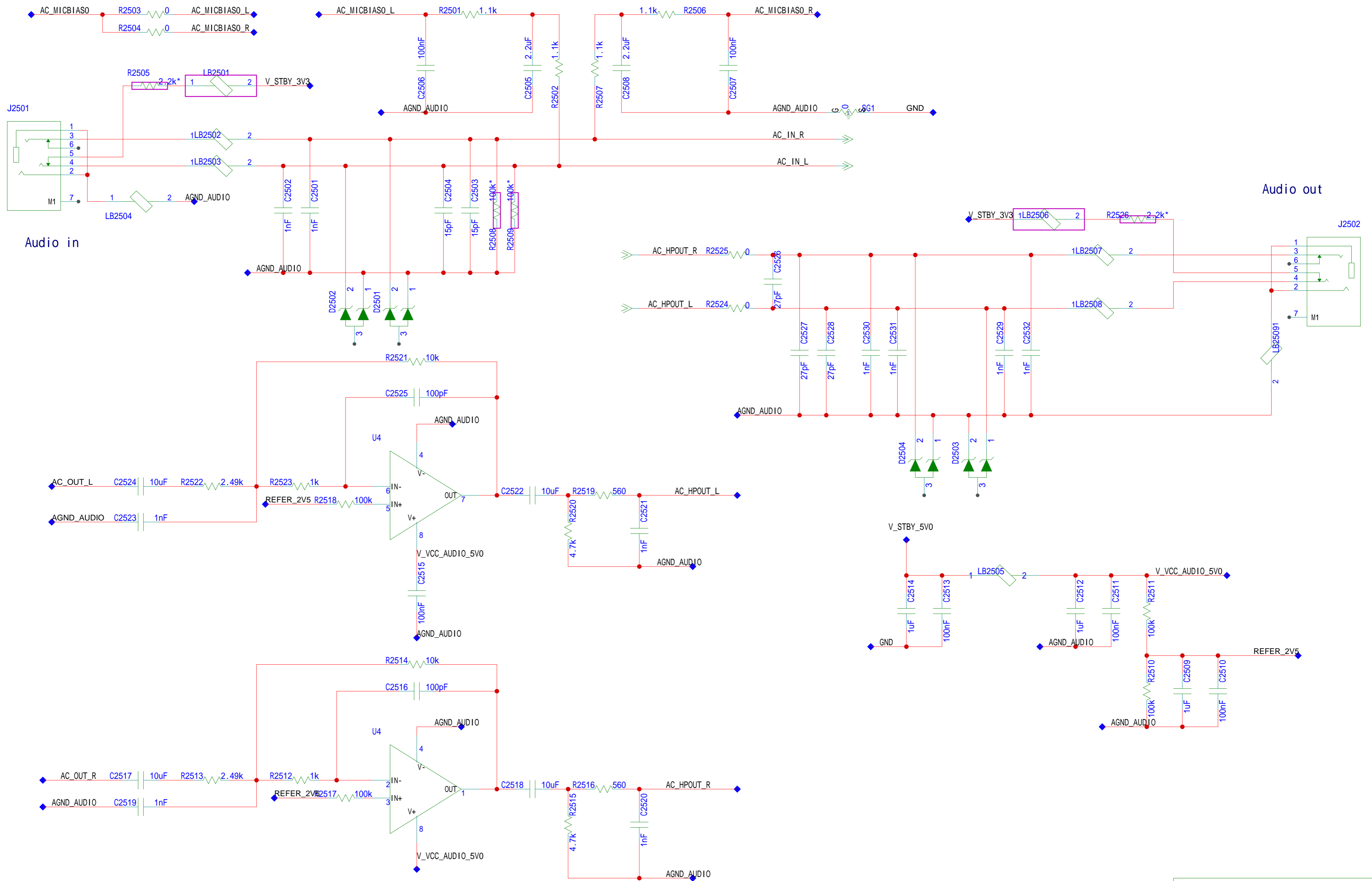
HDMI1 2.0 OUT



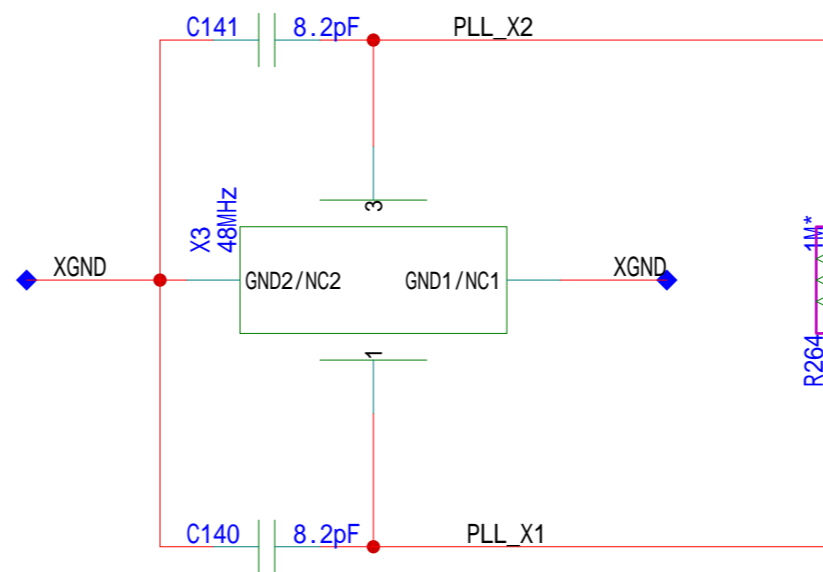
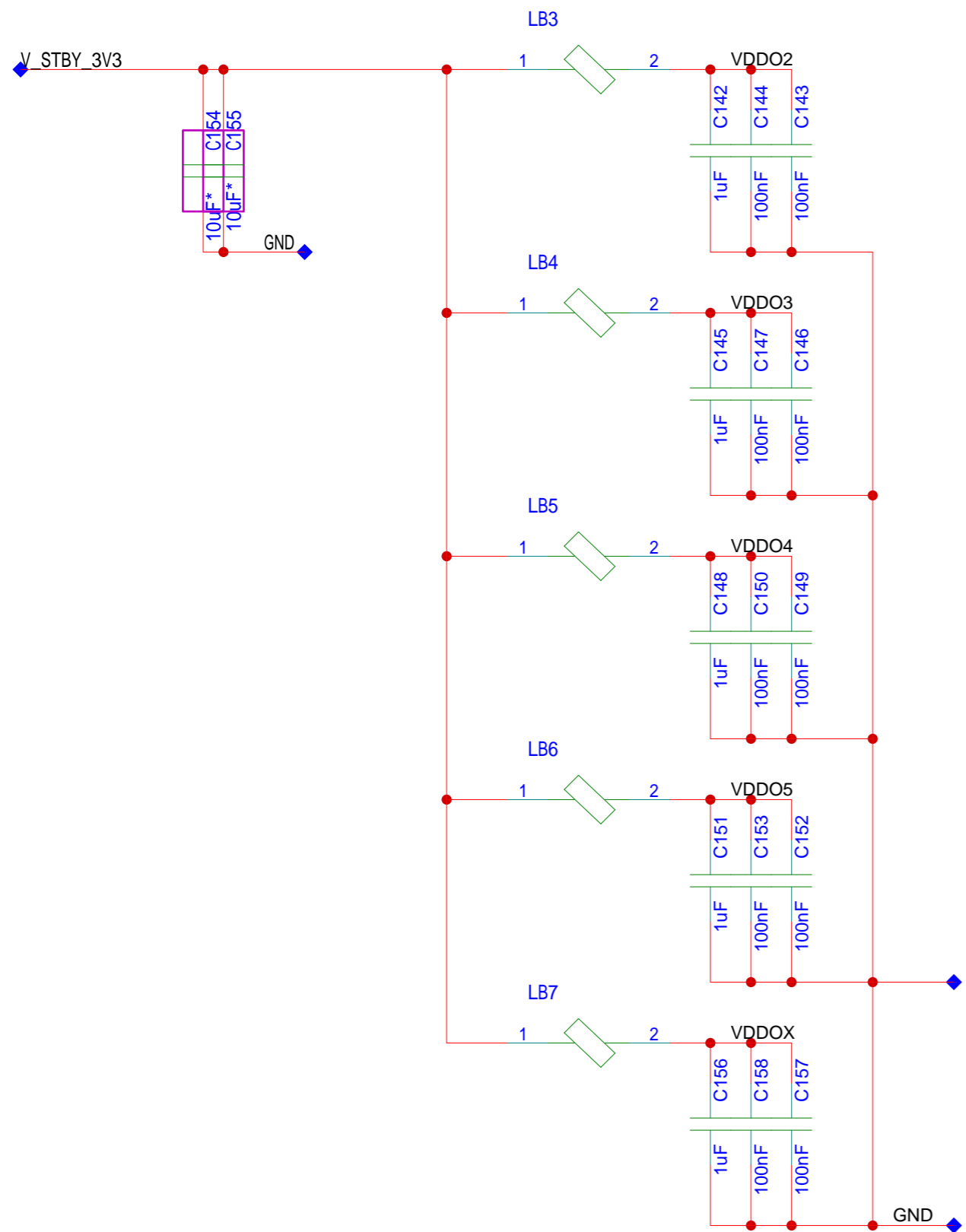
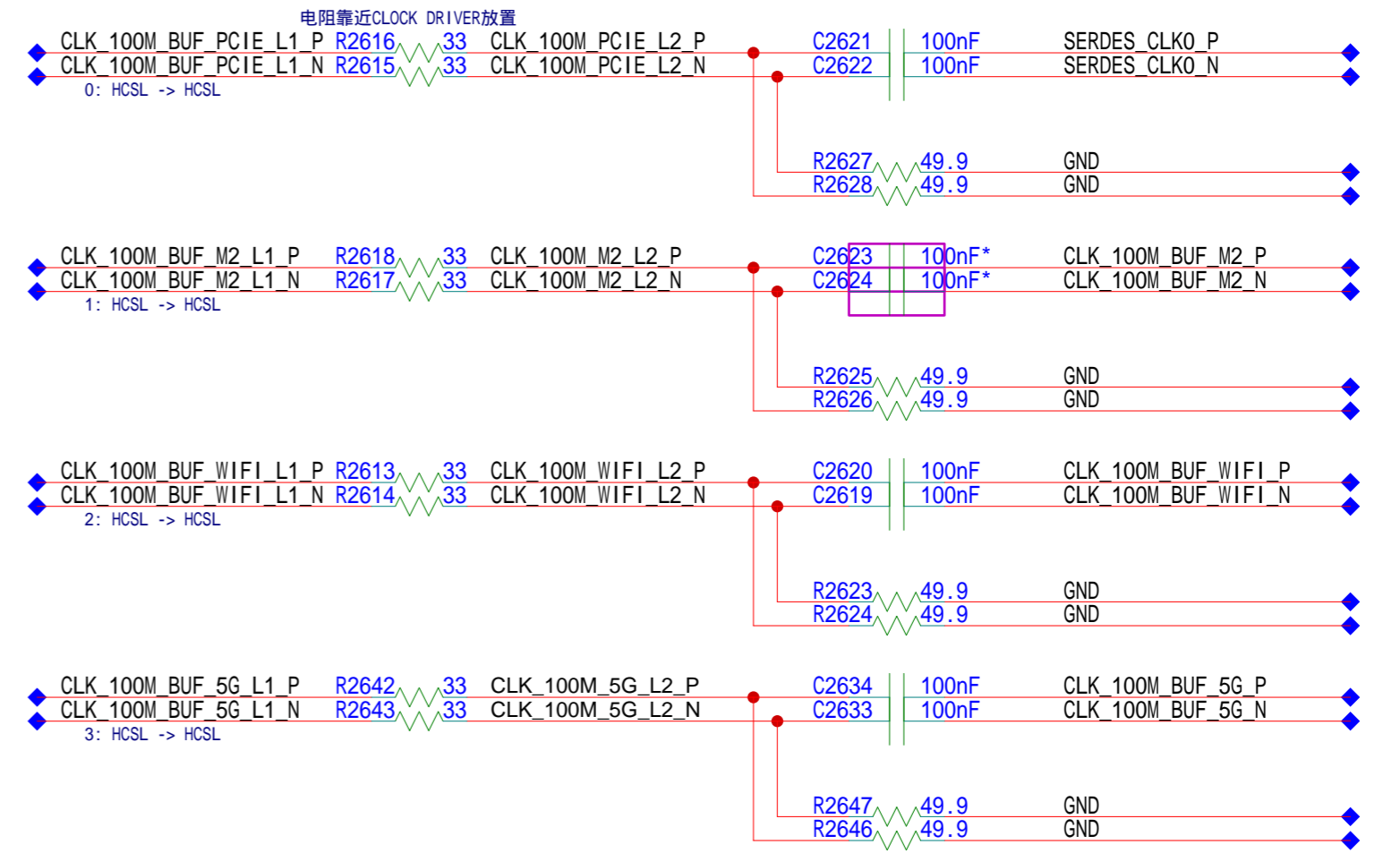
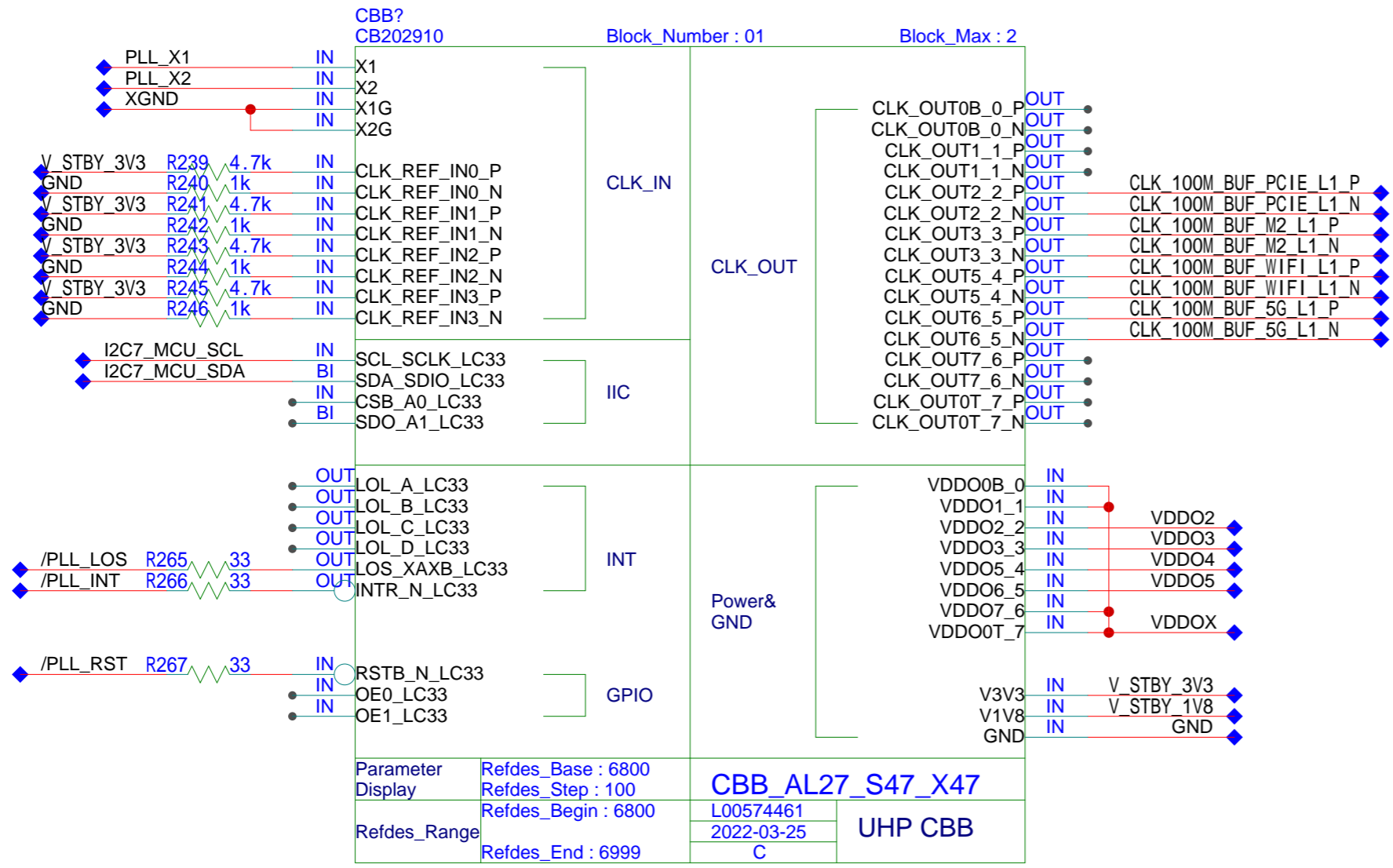
靠近端口侧放置



音频接口



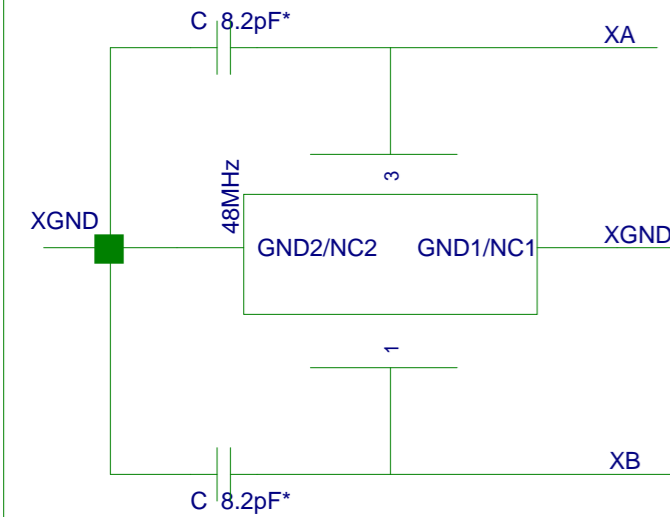
CLOCK



For details about the peripheral circuits of the CBB, see the white block diagram.

NOTE: Huawei internal CBB. Do not discuss with external suppliers or take screenshots. !!

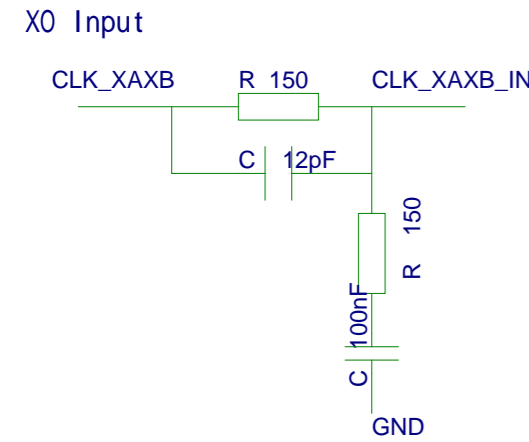
48 MHz crystal is recommended.



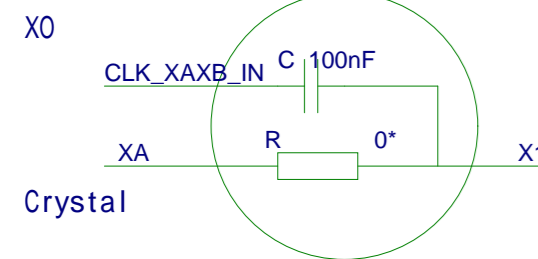
Crystal-compatible crystal oscillator circuit:

Whether the crystal oscillator circuit is reserved depends on product requirements.

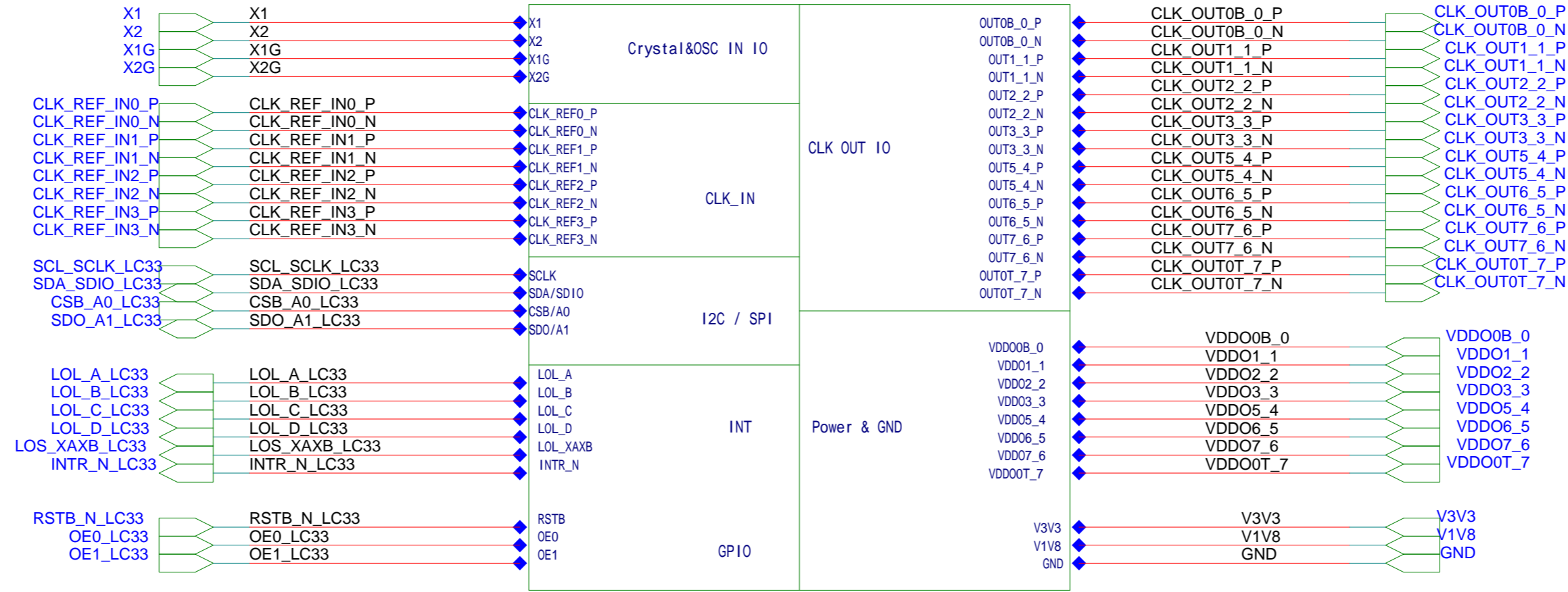
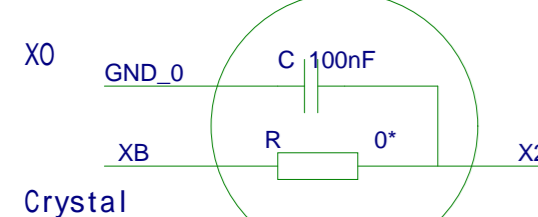
Crystal-compatible crystal oscillator circuit:



Stacked Pad



Stacked Pad



Output Note :

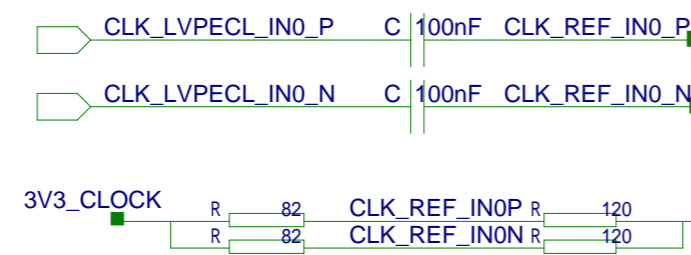
X47 : When the OUT1 pin is used for output, if the output clock frequency ranges from 50 MHz to 90 MHz, the output clock cannot be used as a high-performance clock (HI30/HI60, RMS jitter less than 300 fs) but can be used as a common performance clock (jitter less than 1 ps). There is no restriction on other frequencies.

L27/S47/X47:

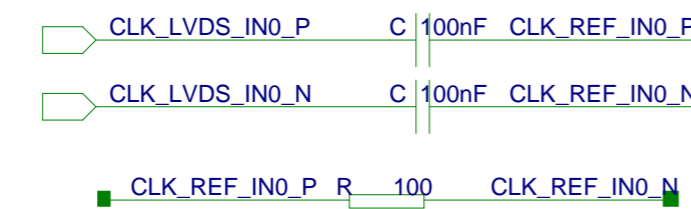
- Generally, it is not recommended to output single-ended clock signals. If different reference sources are used or the output frequency is not multiplied, the single-ended clock output pin must be separated from the differential clock output pin by at least two channels. Otherwise, the output clock performance of the differential pin will be affected (not meeting the H30/H60 requirements). The two differential outputs corresponding to different reference source inputs must be separated by one channel.
- Intra-frequency clocks output by the same loop or clocks with frequency multiplication relationships can be discharged without interval output pins.
- If the same clock source is traced for the same clock output by different loops or the clock with frequency multiplication relationship, the output pins do not need to be spaced.

REF_IN:Reference Circuit

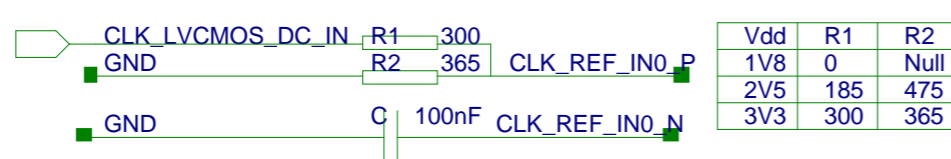
Option1 : AC Coupled Differential LVPECL



Option2 : AC Couple Differential LVDS/LVPECL

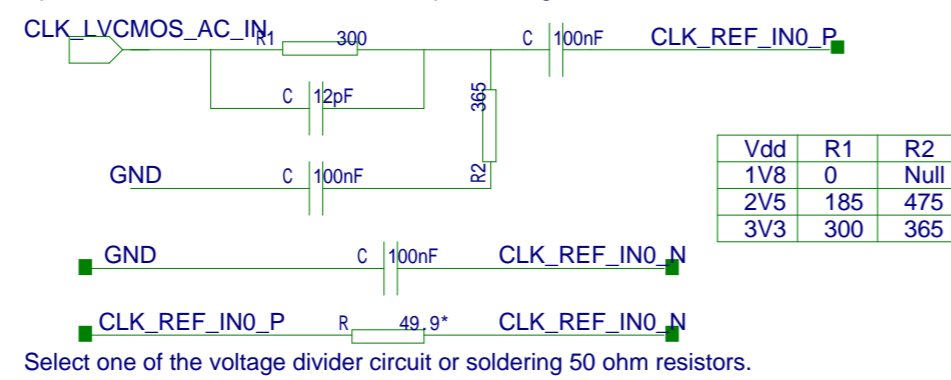


Option3 : Pulsed CMOS DC Coupled Signle Ended



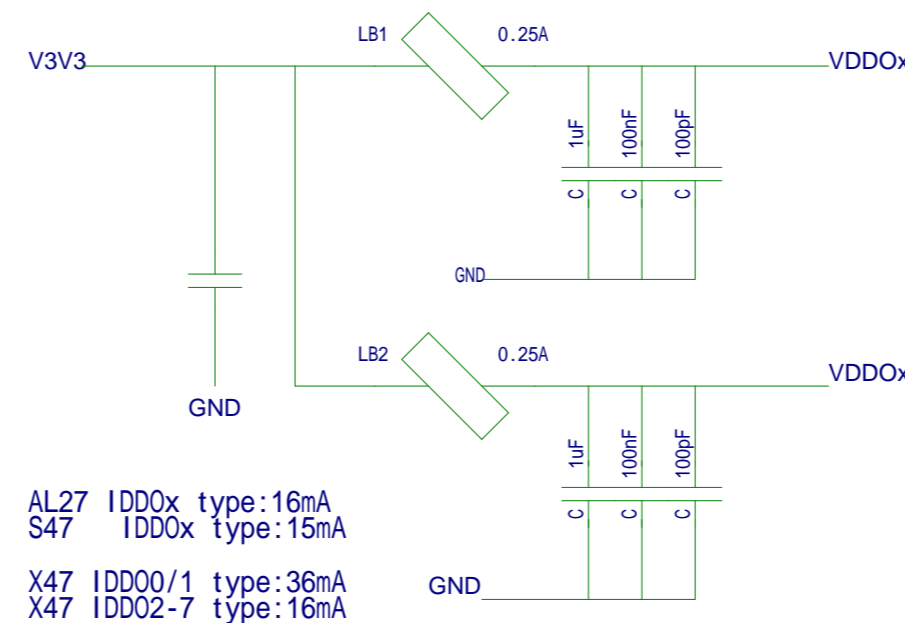
When LVCMOS DC Coupling, please select the appropriate resistance to be compatible with the requirements of the co-coding chip for the single-ended DC input
 AL27 LVCMOS DC Vih higher than 0.8V S47 LVCMOS DC Vih higher than 0.8V
 X47 LVCMOS DC Vih higher than 0.9V

Option4 : Pulsed CMOS AC Coupled Signle Ended



VDDOx:Reference Filter Circuit

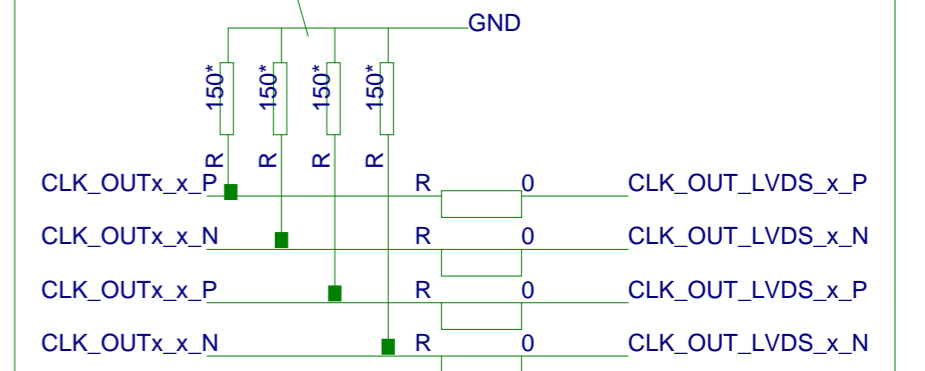
Each product designs its own VDDOx circuit as needed



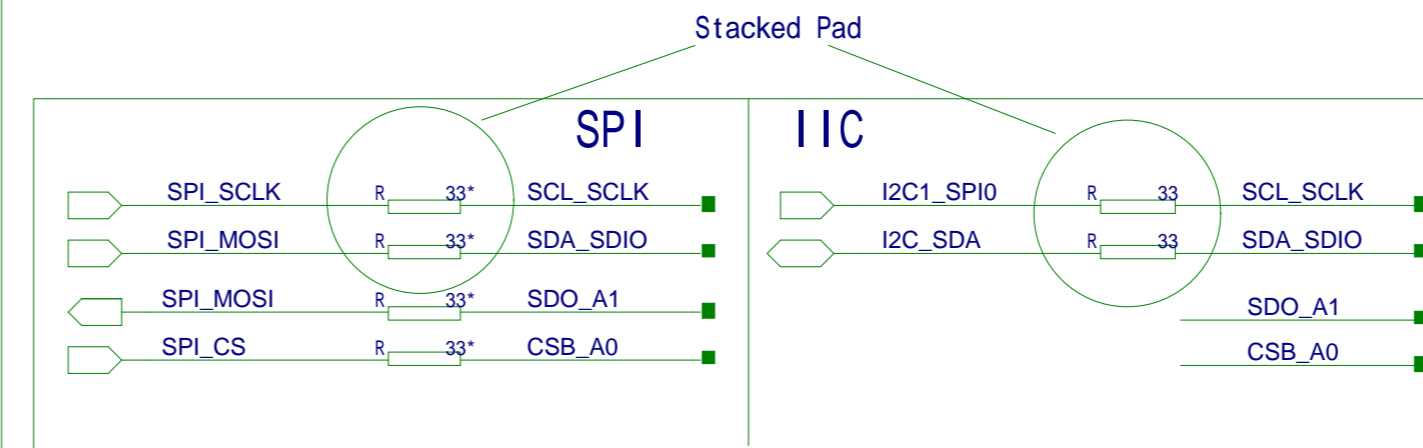
CLK_OUT:Reference Circuit

Option for Diff Output

The 150 ohm resistor is only used in LVPECL2 mode of AL53x7



NOTE:It is recommended to use LVDS output string 0 ohm resistor



CLOCK CBB - 1

CLOCK CBB -2

NOTE: Huawei internal CBB. Do not discuss with external suppliers or take screenshots. ! ! !

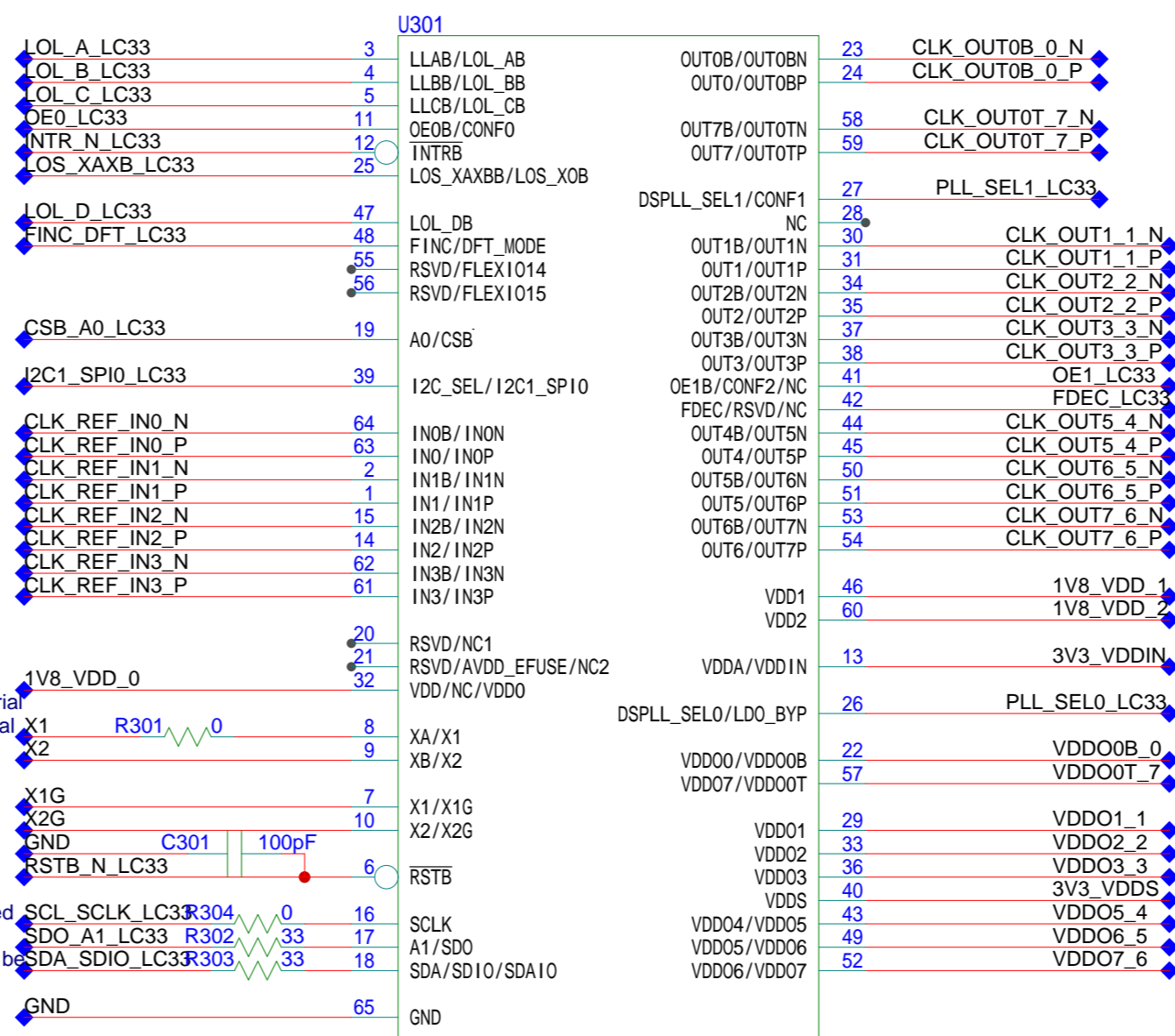
Compatible with S47 and AL27 and X47

PIN	S47	AL27	X47
3	LOL_A	LOL_A	LOL_A
4	LOL_B	LOL_B	LOL_B
5	LOL_C	LOL_C	LOL_C
11	OE0b	OE0b	OE0b
12	INTR	INTR	INTR
25	LOS_XAXB	LOS_XOB	LOS_XAXB
47	LOL_D	LOL_D	LOL_D
48	FINC	FINC	FINC
55	RSVD	FLEXIO14	RSVD
56	RSVD	FLEXIO15	RSVD
19	CSb/A0	CSb	CSb/A0
39	I2C_SEL	I2C1_SPI0	I2C_SEL
64	IN0b	IN0N	IN0b
63	IN0	IN0P	IN0
2	IN1b	IN1N	IN1b
1	IN1	IN1P	IN1
15	IN2b	IN2N	IN2b
14	IN2	IN2P	IN2
62	IN3b	IN3N	IN3b
61	IN3	IN3P	IN3
20	RSVD	NC	RSVD
21	RSVD	NC	RSVD
32	VDD	NC	VDD
8	XA	X1	XA
9	XB	X2	XB
7	X1	X1G	X1
10	X2	X2G	X2
6	RSTb	RSTB	RSTb
16	SCLK	SCLK	SCLK
17	SDO/A1	SDO	SDO/A1
18	SDA/SDIO	SDAIO	SDA/SDIO
65	GND	GND	GND

PIN	Pin Differences
11 OE0b	This pin is not used in normal applications of the three chips and requires pull-down. For S47 and L27, this pin controls the output enable of all outputs. For X47, this pin can control all output enable status only after this pin is enabled in the register.
19 CSb/A0	L27 does not support the 3-wire SPI mode. Both X47 and S47 support the 3-wire SPI mode. L27 does not support continuous reading and writing of multiple registers in SPI mode. Both X47 and S47 support this function. L27 does not support continuous writing of multiple registers in IIC mode. Both X47 and S47 support writing this pin is the same for the normal application of the three chips.
40 VDDS	The X47 pin has no actual function and can be connected or not. When the chip of other vendors is compatible, the 3V3 power supply must be connected. S47 This pin determines the VIH/VIL level of the FDEC and OE1b. It must be connected to the 3V3 power supply. L27: This pin determines the VIH/VIL level of the FDEC. It must be connected to the 3V3 power supply.
41 OE1b	This pin is not used in normal applications of the three chips and requires pull-down. S47: This pin works with OE1a to enable or disable the chip output. L27: This pin is not used.
55 RSVD	For X47, this pin can control all output enable status only after this pin is enabled in the register.
56 RSVD	This pin is not used when the three chips are normally used. The pin is pulled up or floated.
5 FLEX	For S47 and X47, this pin has no function. For L27, this pin can be used as a FLEX pin.
6 FLEX	This pin is not used when the three chips are normally used. The pin is pulled up or floated. For S47 and X47, this pin has no function. For L27, this pin can be used as a FLEX pin.

X1: This 0 ohm adjusts the serial resistance to prevent the crystal from being overexcited.

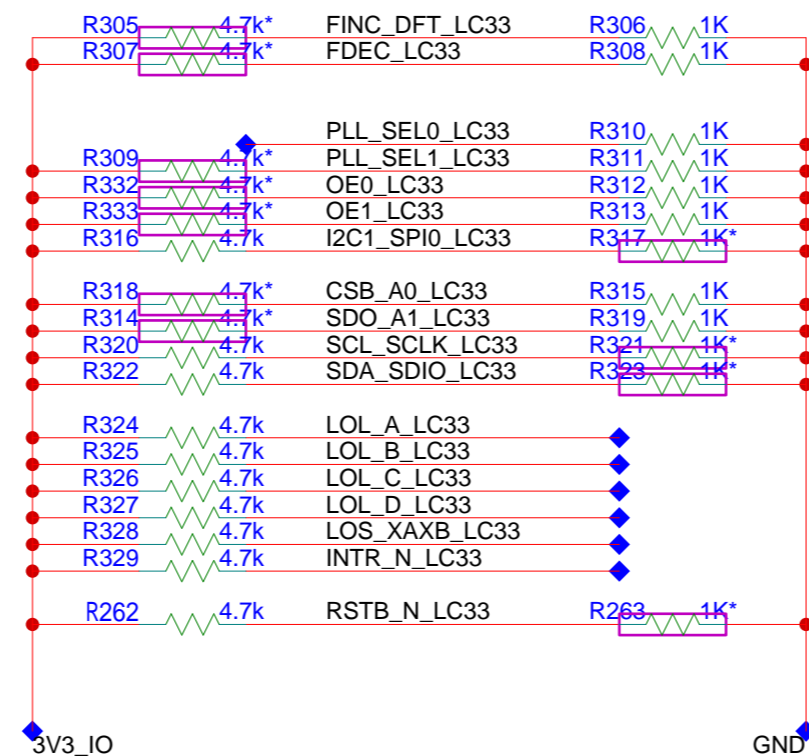
SCL_SCLK: This 0 ohm is used to adjust the signal quality. It is recommended that this 0 ohm be placed near the source end.



PIN	S47	AL27	X47
23	OUT0b	OUT0BN	OUT0b
24	OUT0	OUT0BP	OUT0
58	OUT7b	OUT0TN	OUT7b
59	OUT7	OUT0TP	OUT7
27	DSPLL_SEL1	PLL_SEL1	DSPLL_SEL1
28	NC	NC	NC/RSVD
30	OUT1b	OUT1N	OUT1b
31	OUT1	OUT1P	OUT1
34	OUT2b	OUT2N	OUT2b
35	OUT2	OUT2P	OUT2
37	OUT3b	OUT3N	OUT3b
38	OUT3	OUT3P	OUT3
41	OE1b	NC	OE1b
42	FDEC	FDEC	FDEC
44	OUT4b	OUT5N	OUT4b
45	OUT4	OUT5P	OUT4
50	OUT5b	OUT6N	OUT5b
51	OUT5	OUT6P	OUT5
53	OUT6b	OUT7N	OUT6b
54	OUT6	OUT7P	OUT6
46	VDD	VDD	VDD1
60	VDD	VDD	VDD2
13	VDDA	VDDIN	VDDA
26	DSPLL_SEL_0	PLL_SEL_0	DSPLL_SEL_0
22	VDDO0	VDDO0B	VDDO0
57	VDDO7	VDDO7	VDDO7
29	VDDO1	VDDO1	VDDO1
33	VDDO2	VDDO2	VDDO2
36	VDDO3	VDDO3	VDDO3
40	VDDO4	VDDO4	VDDO4
43	VDDO5	VDDO5	VDDO5
49	VDDO6	VDDO6	VDDO6
52	VDDO6	VDDO7	VDDO6

Functions of GPIO pins:

FINC/FDEC	X47/S47/AL27:FINC , Used as frequency up step control in DCO mode X47/S47/AL27:FDEC , Used as frequency down step control in DCO mode
PLL_SELO/1	X47/S47/AL27:PLL_SELO with PLL_SEL1 , Loop selection signal for pin control in DCO mode
OE1/OE2	X47/S47/AL27: OE1 works with OE2 to determine all output configurations of the chip.X47/S47/AL27: Pull-down resistors must be connected to the ground. Pull-up resistors cannot be connected or floated.The pull-up resistors in the circuit must be soldered and reserved. Note that the X47 can be used only after the register is configured.
I2C1_SPI0	I2C_SEL=1 : IIC mode; I2C_SEL=0 SPI mode Pull-up IIC mode and pull-down SPI mode. The IIC mode is recommended.
A0/A1	A0: used as the A0 address in IIC mode and as the chip select pin in SPI mode. Internal pull-up, floating when not in use. A1: used as the A1 address in IIC mode and as the 4-wire SPI data output pin in SPI mode;
LOL_A/B/C/D	SDAIO: SDA in IIC mode; bi-direction data in 3-wire SPI mode; data input in 4-wire SPI mode LOLA: PLLA loop lock status interrupt indication signal. It is recommended that this signal be connected to the logic. LOLB: PLLB loop lock status interrupt indication signal. It is recommended that this signal be connected to the logic. LOLC: PLLC loop lock status interrupt indication signal. It is recommended that this signal be connected to the logic. LOLD: PLLD loop lock status interrupt indication signal. It is recommended that this signal be connected to the logic. LOL_XAXB: LOS interrupt indication signal of the XAXB working clock. It is recommended that this signal be connected to the logic.
SCLK/SDAIO	
INTRb	INTRb: interrupt indication signal. It is recommended that this signal be connected to the logic.
RSTB	Reset signal, active low; The logic must be connected. Before the chip is initialized, reset and deassert the reset.

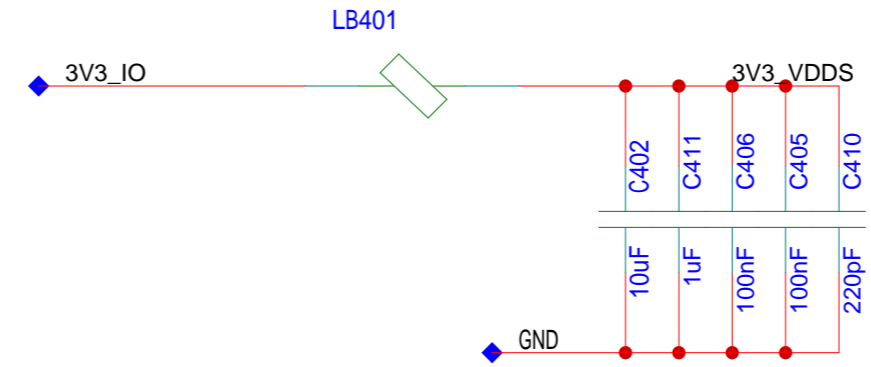
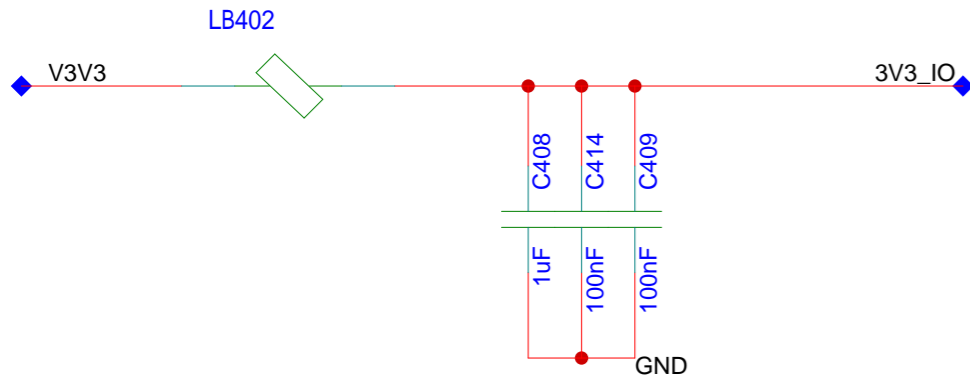


Note: The SPI bus cannot be connected to multiple chips.

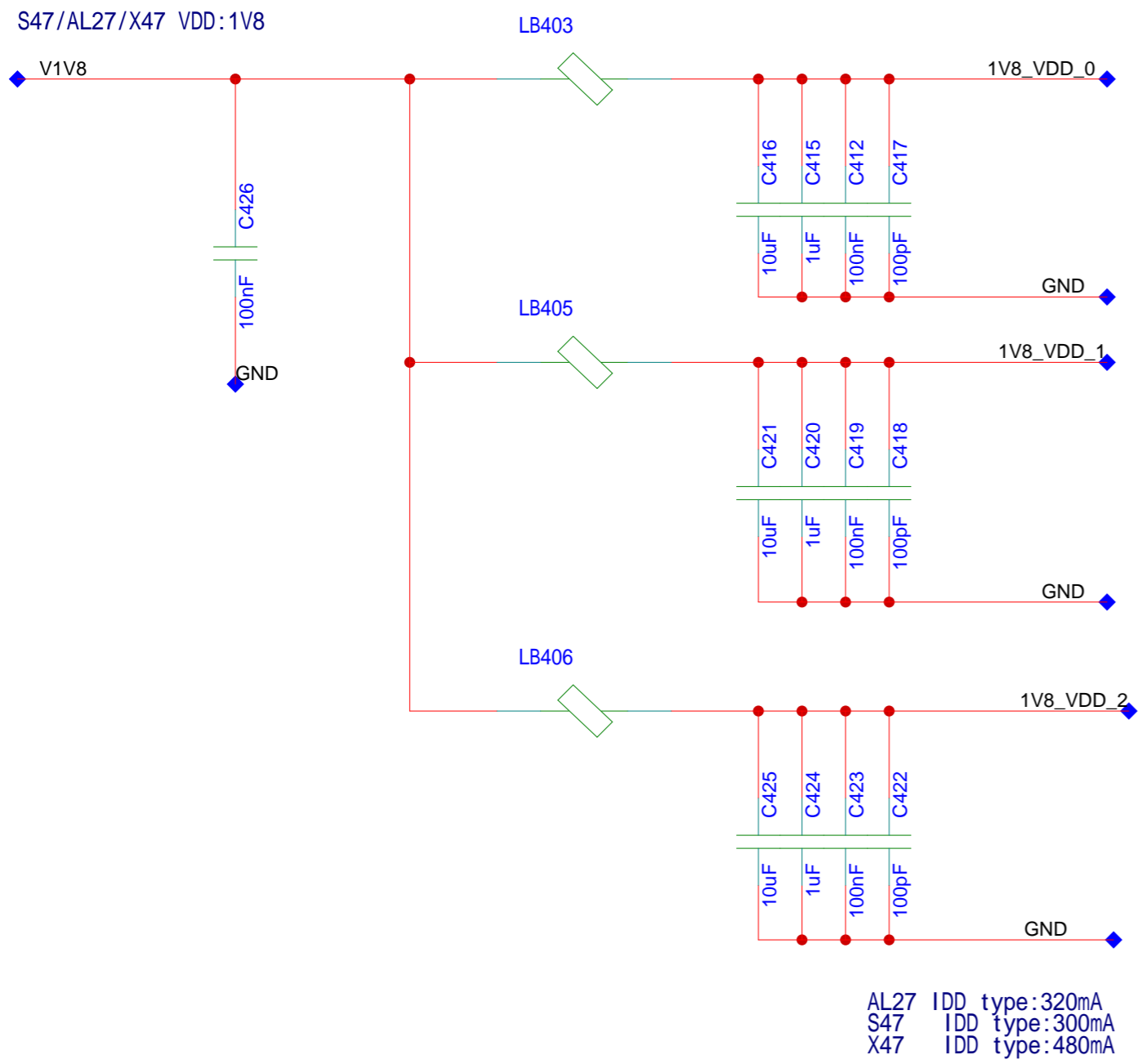
CLOCK CBB -3

Recommended circuit for VDD:

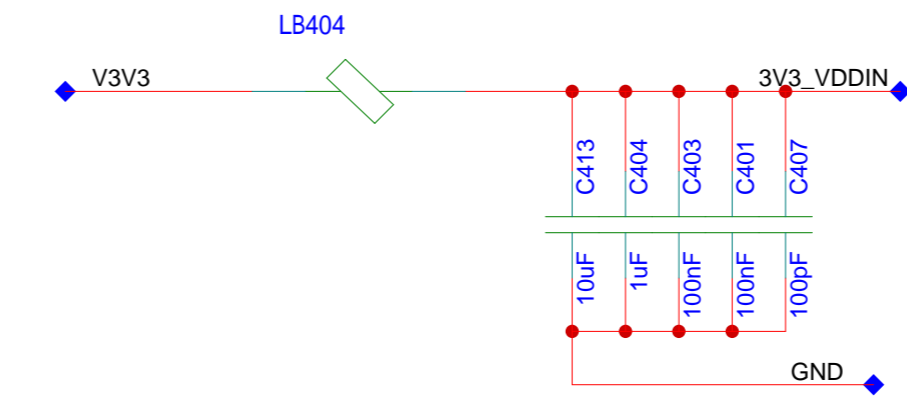
S47/AL27/X47 GPIOs use 3V3 pull-up.



S47/AL27/X47 VDD:1V8

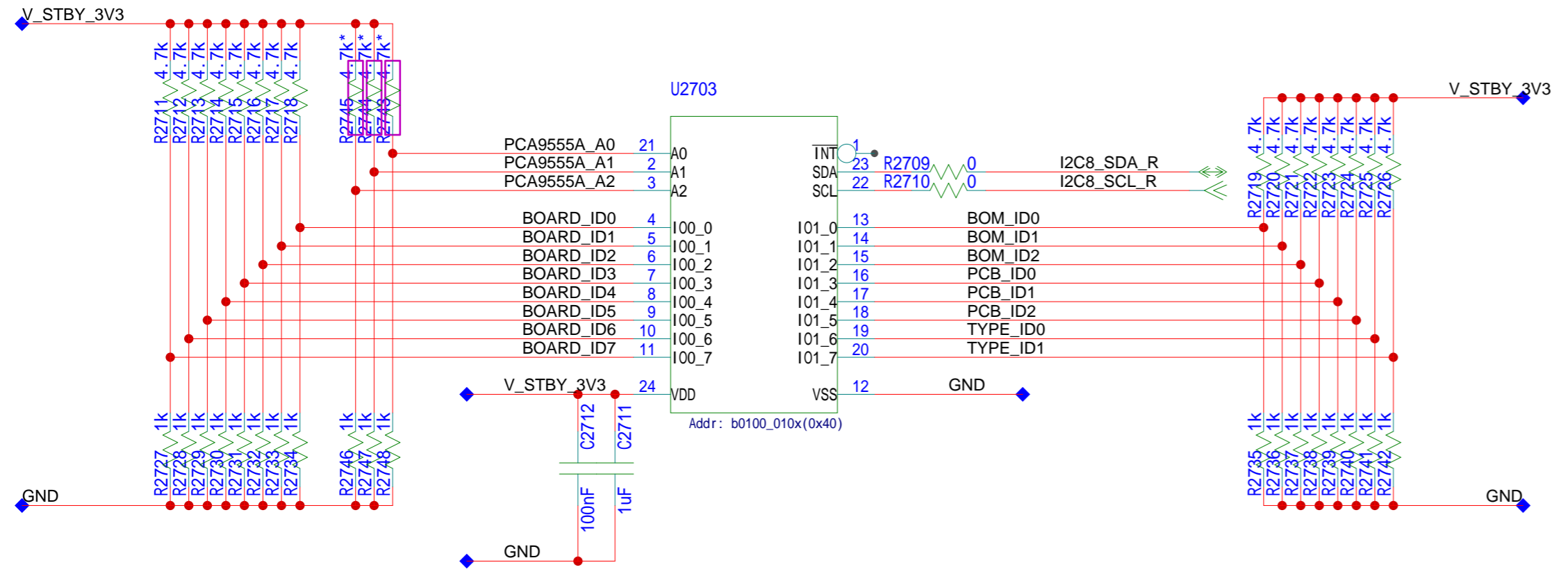
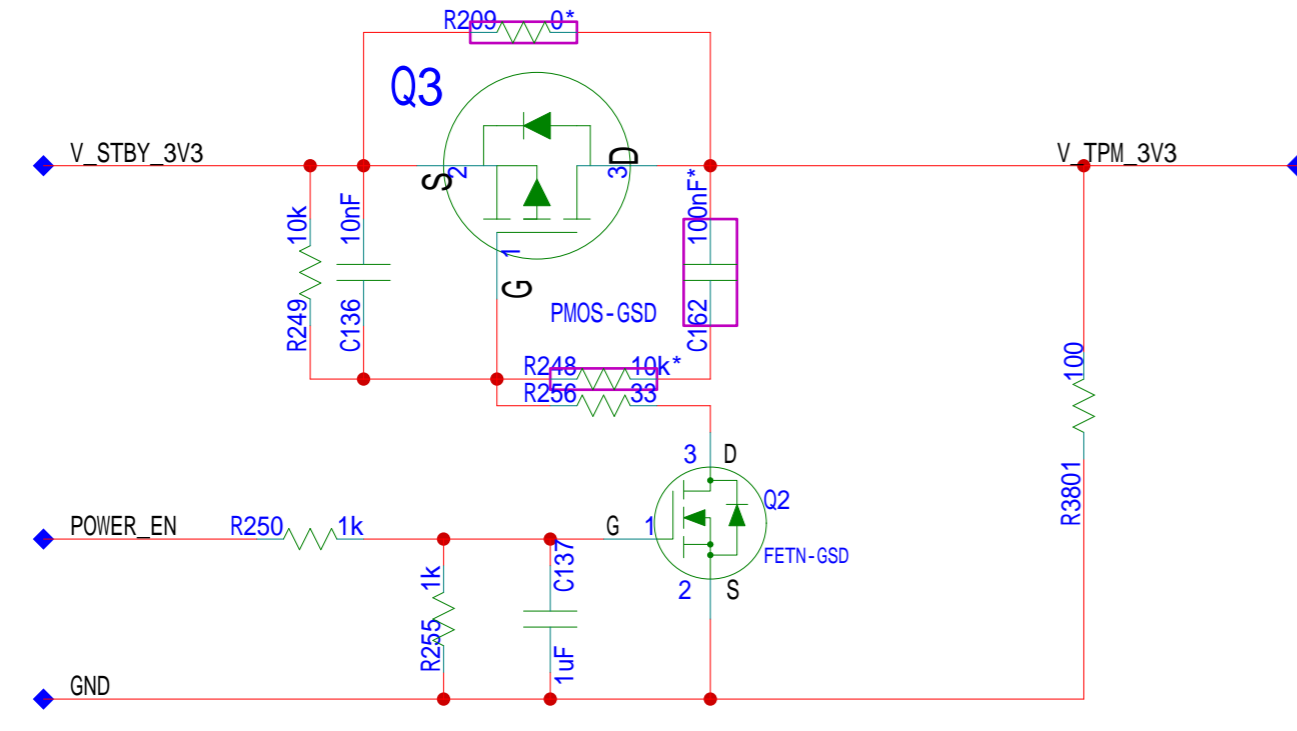
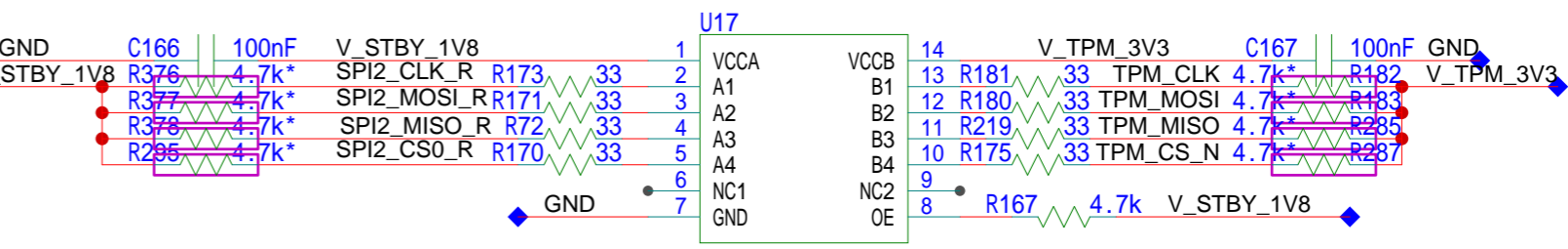
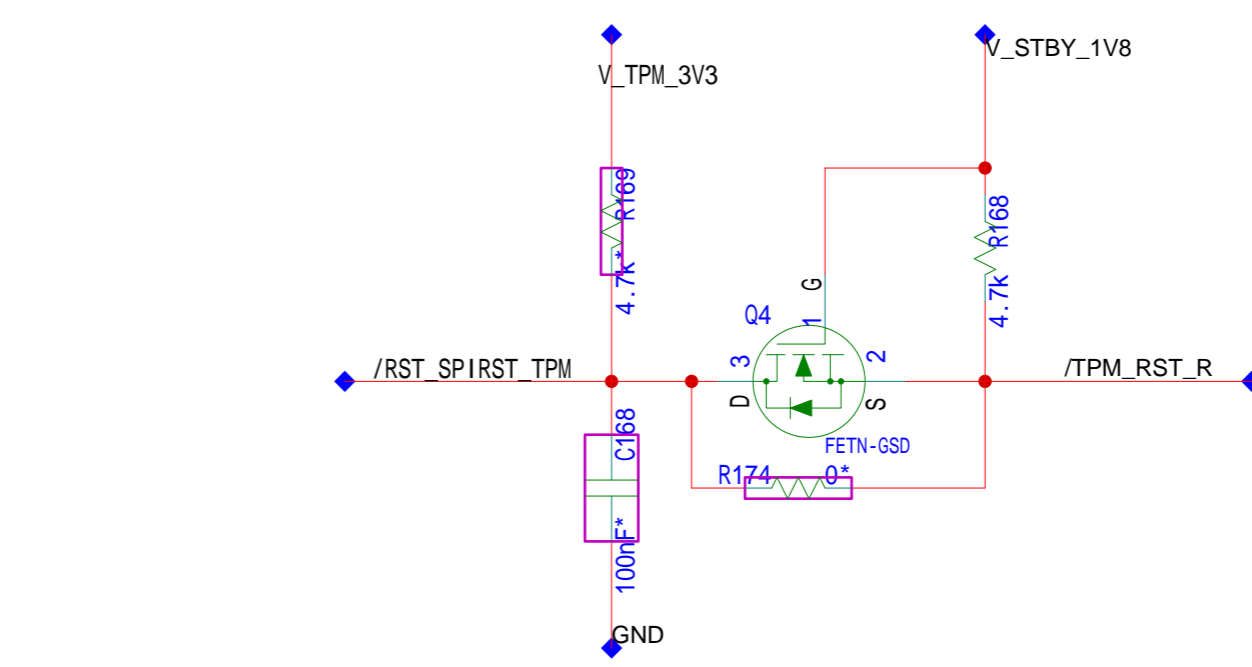
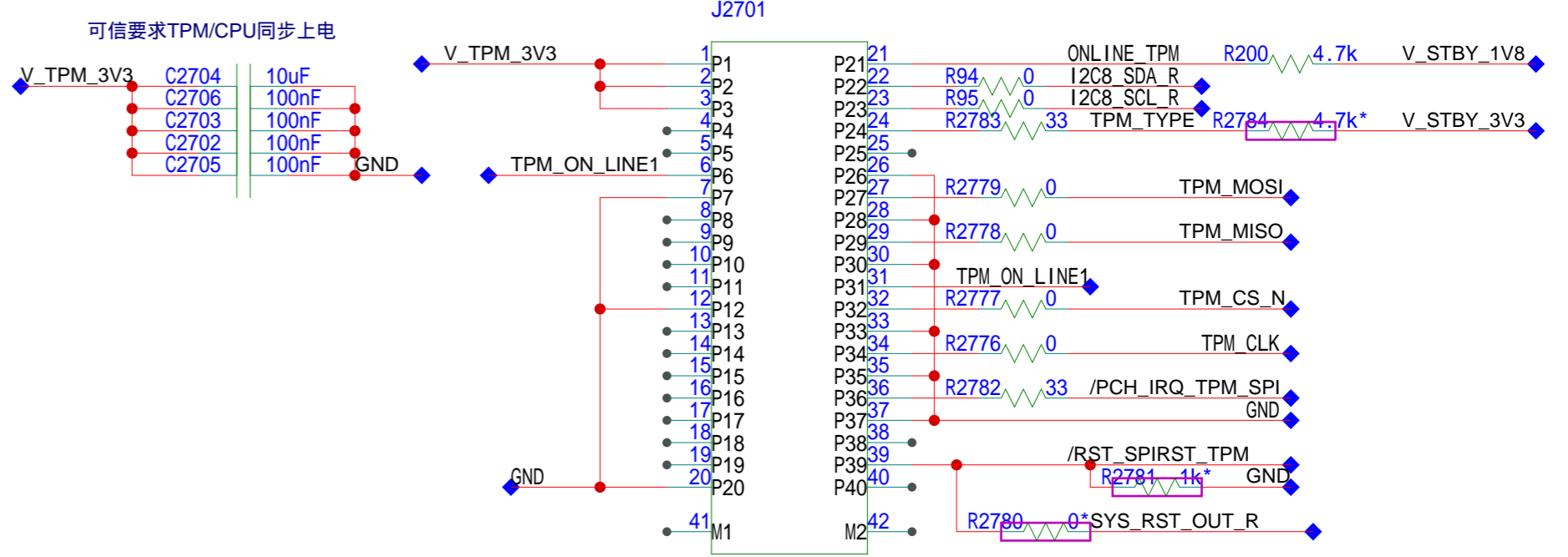
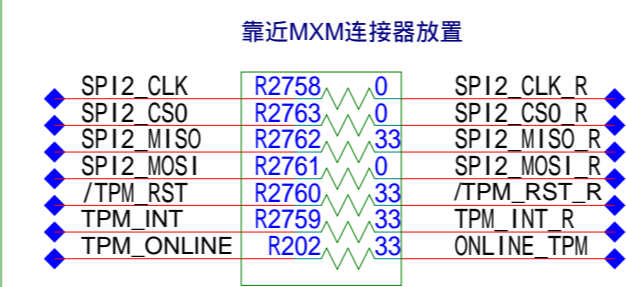
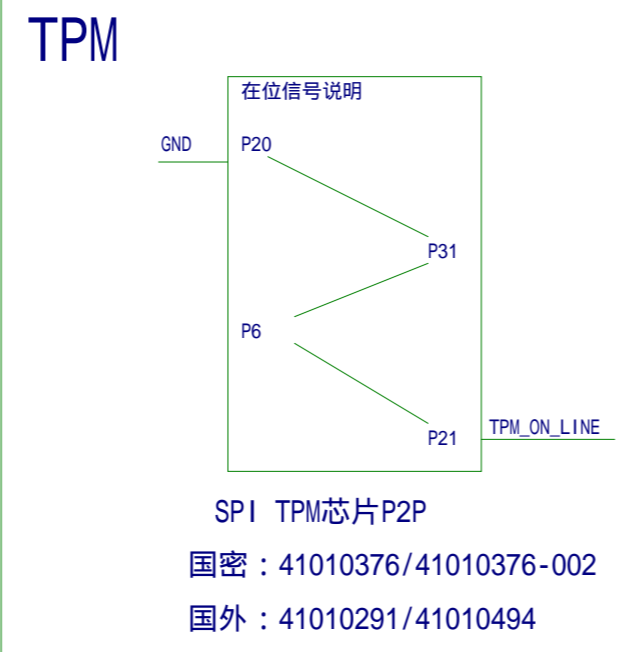
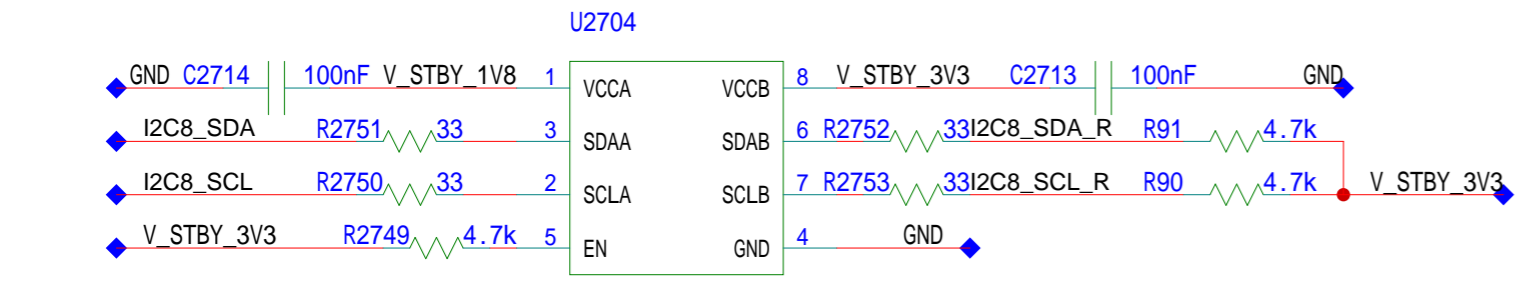
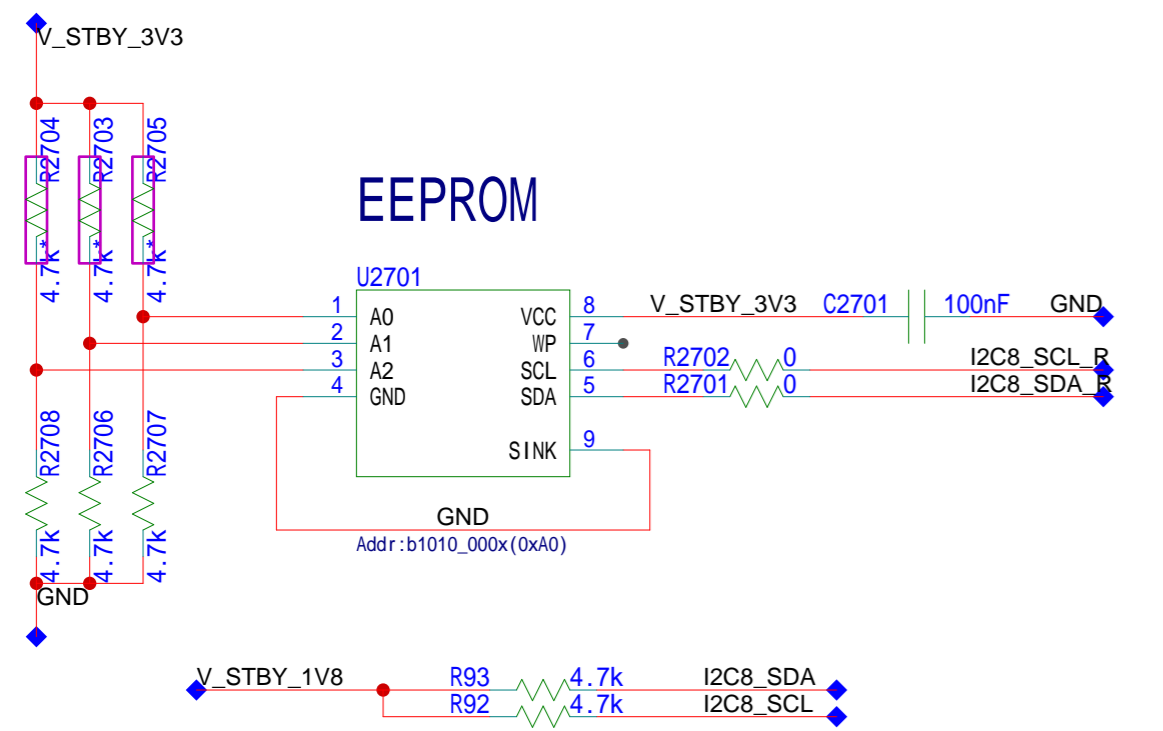


AL27 IDD type:320mA
 S47 IDD type:300mA
 X47 IDD type:480mA

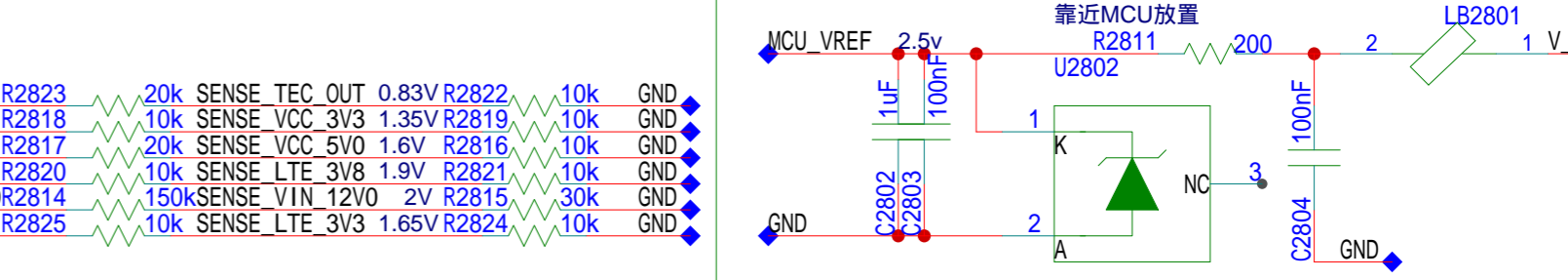
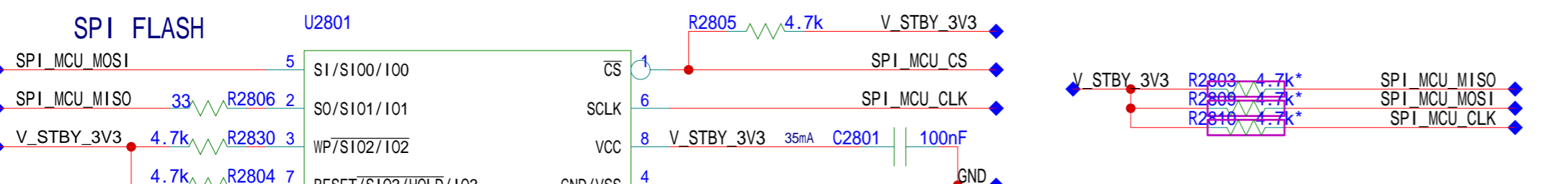
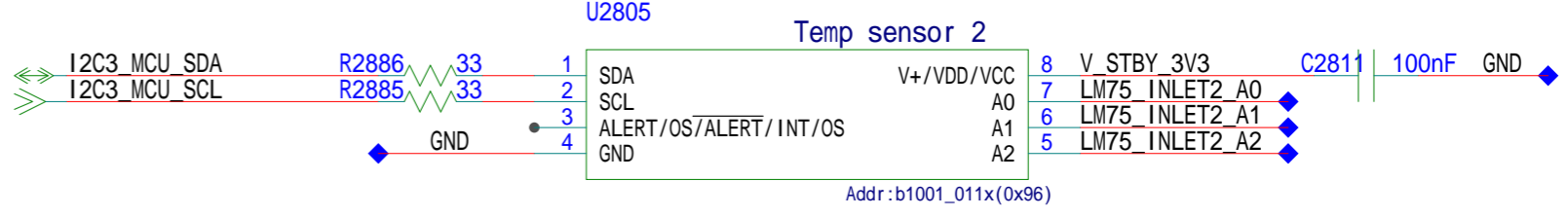
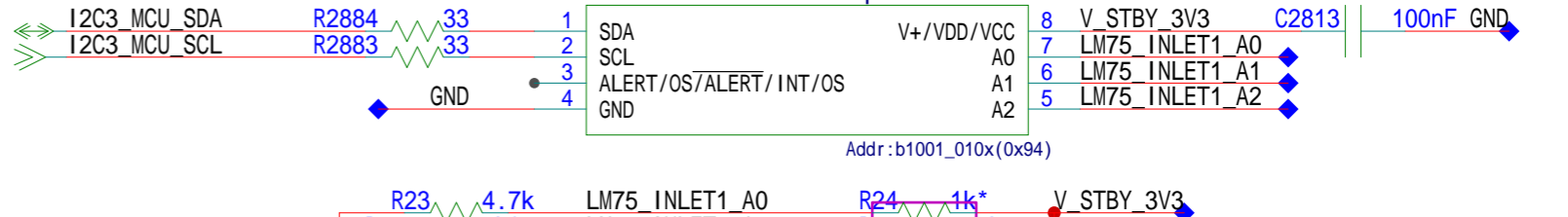
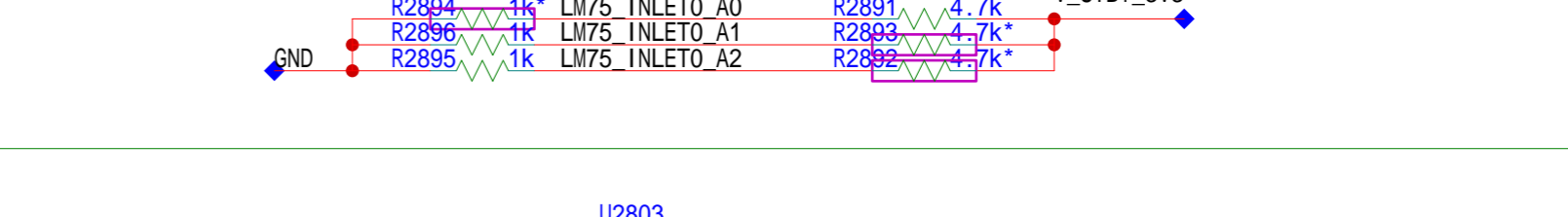
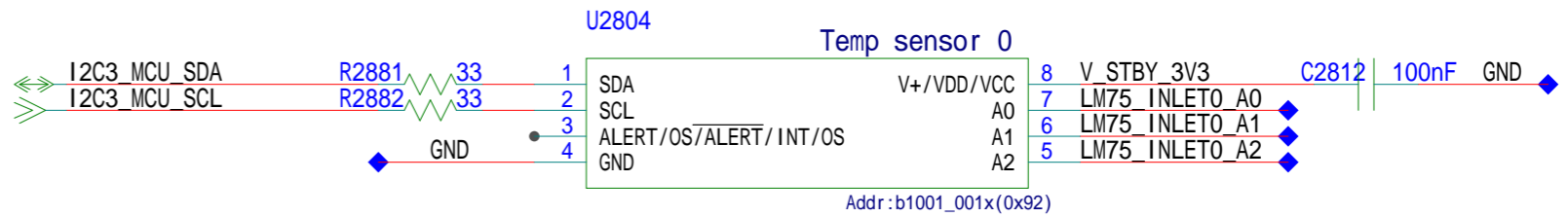
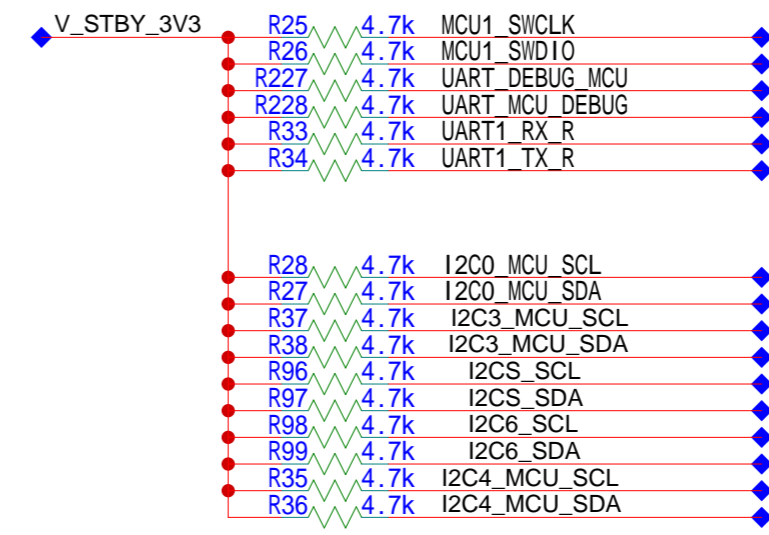
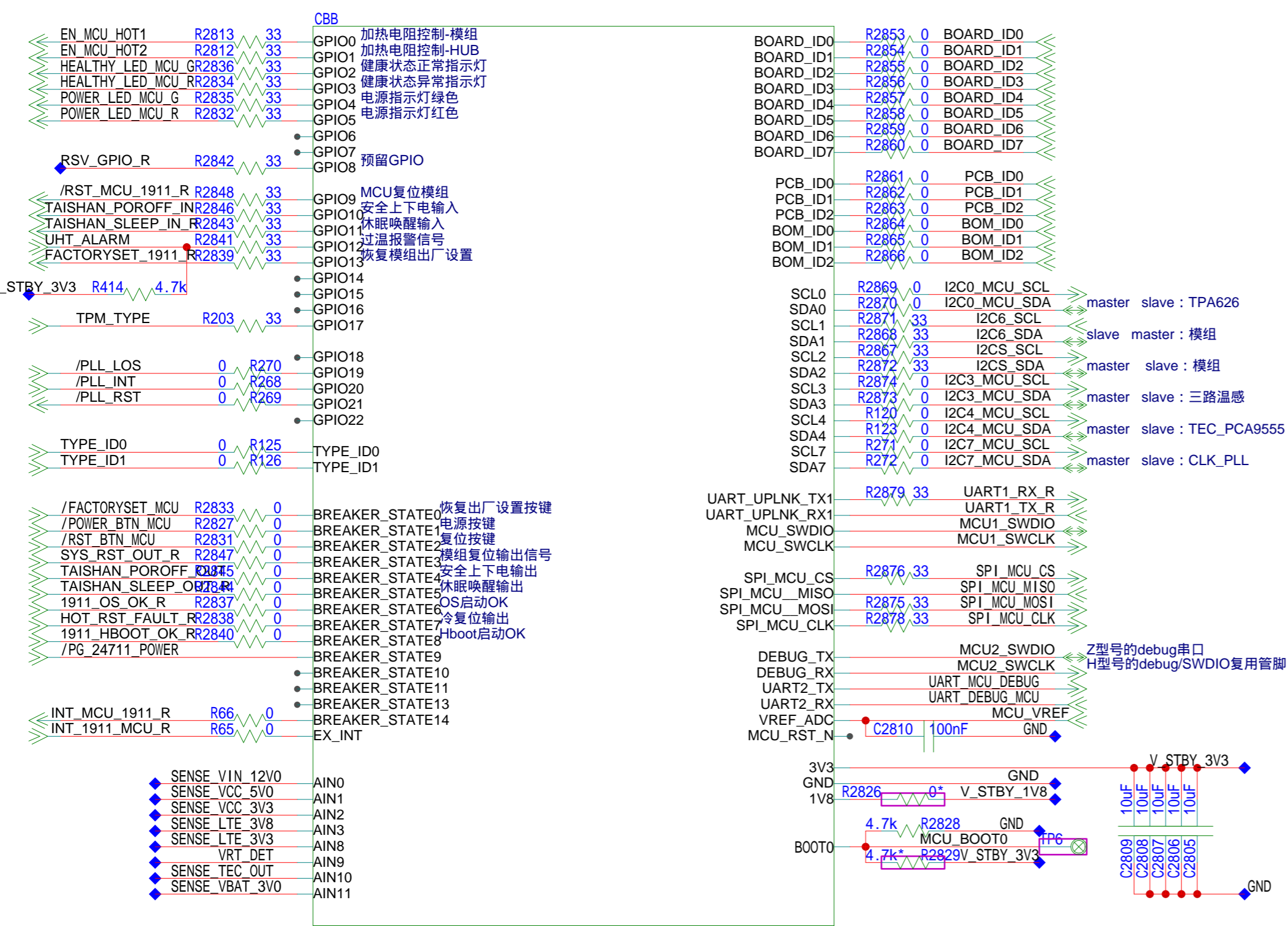


AI27IDDIN type:18mA
 S47 IDDIN type:125mA
 X47 IDDIN type:70mA

Note: Pins 32, 46, and 60 use independent filter circuits. It is recommended that 100 nF capacitors be placed close to each pin on the PCB.



MCU



1

2

3

4

5

6

MCU CBB -1

A

A

B

B

C

C

D

D

MCU CBB电路

1

2

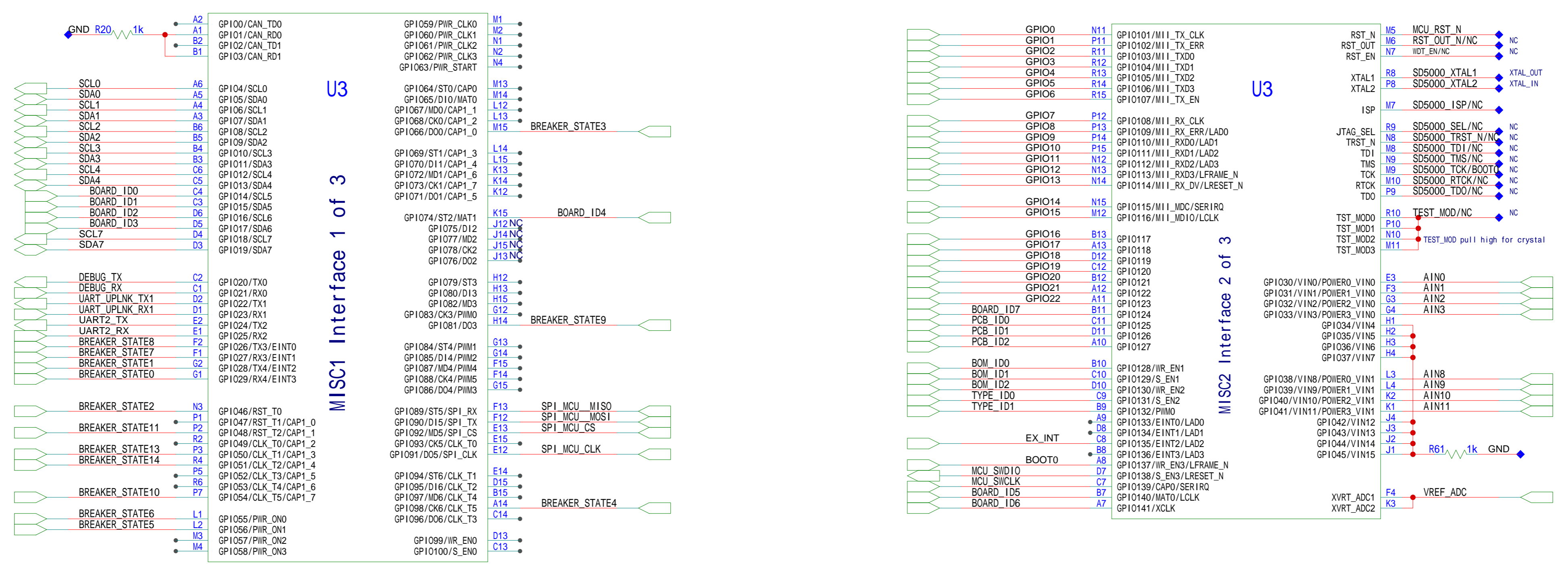
3

4

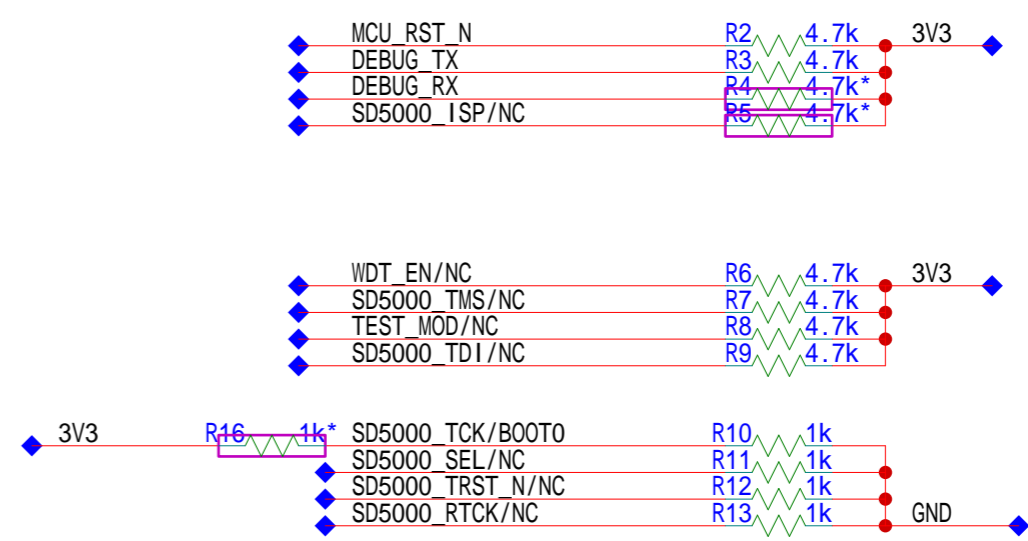
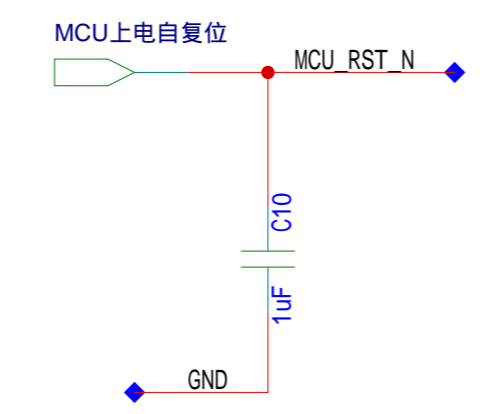
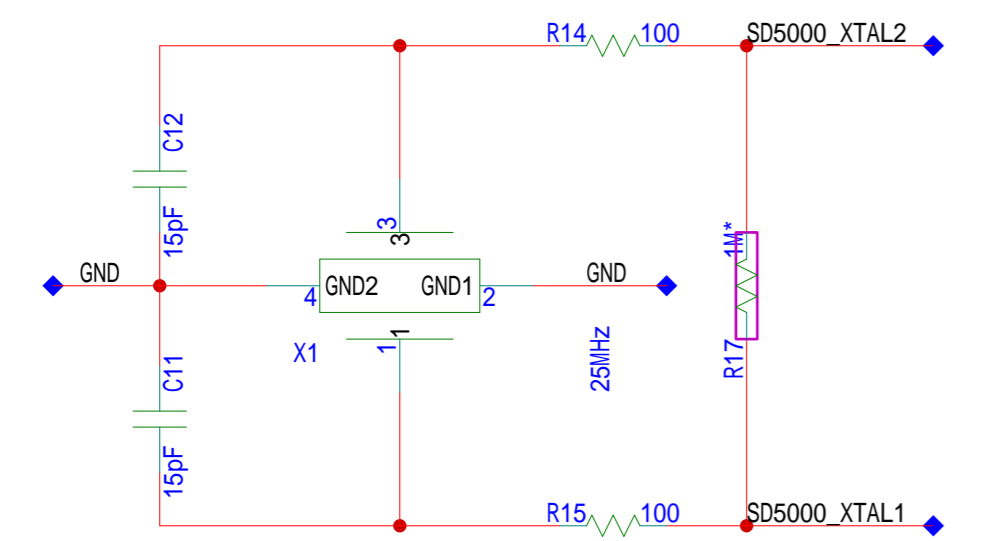
5

6

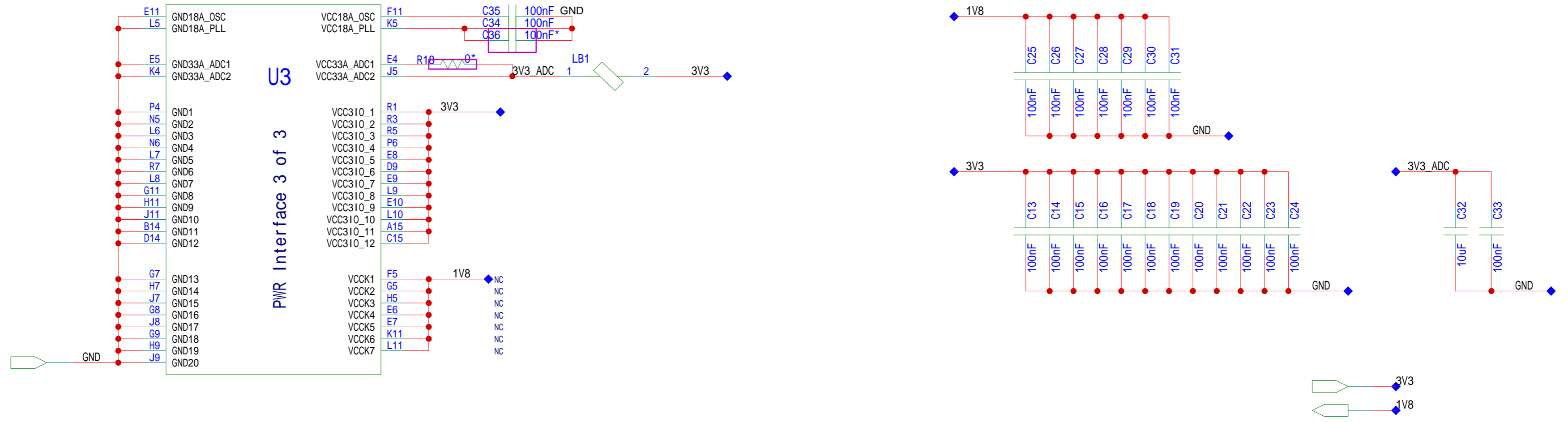
MCU CBB -2



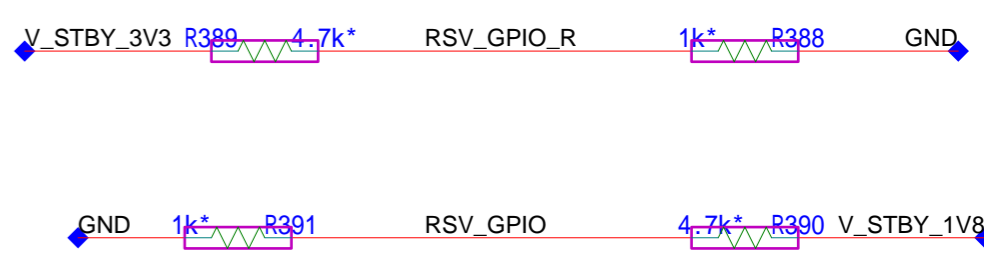
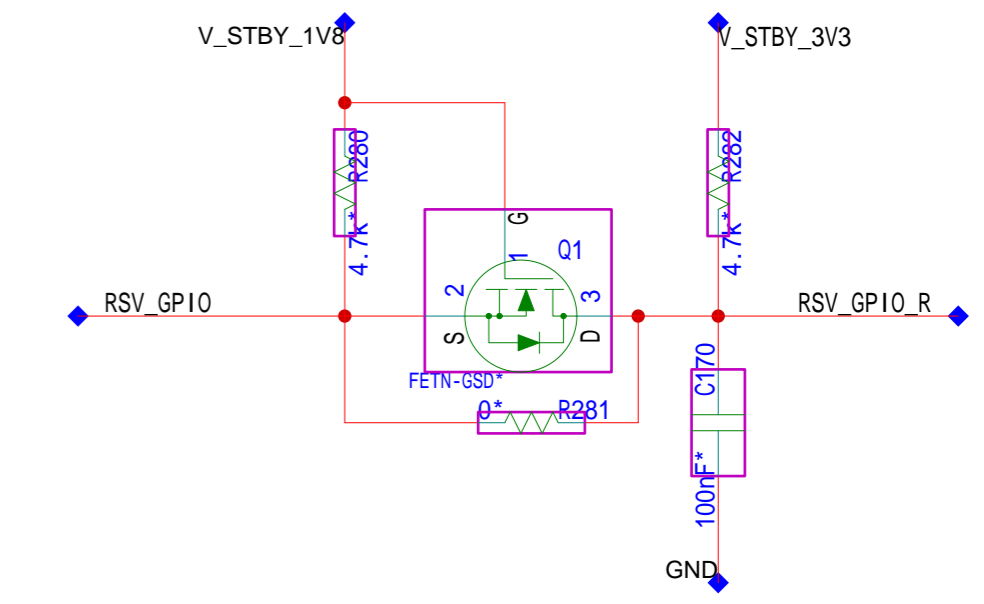
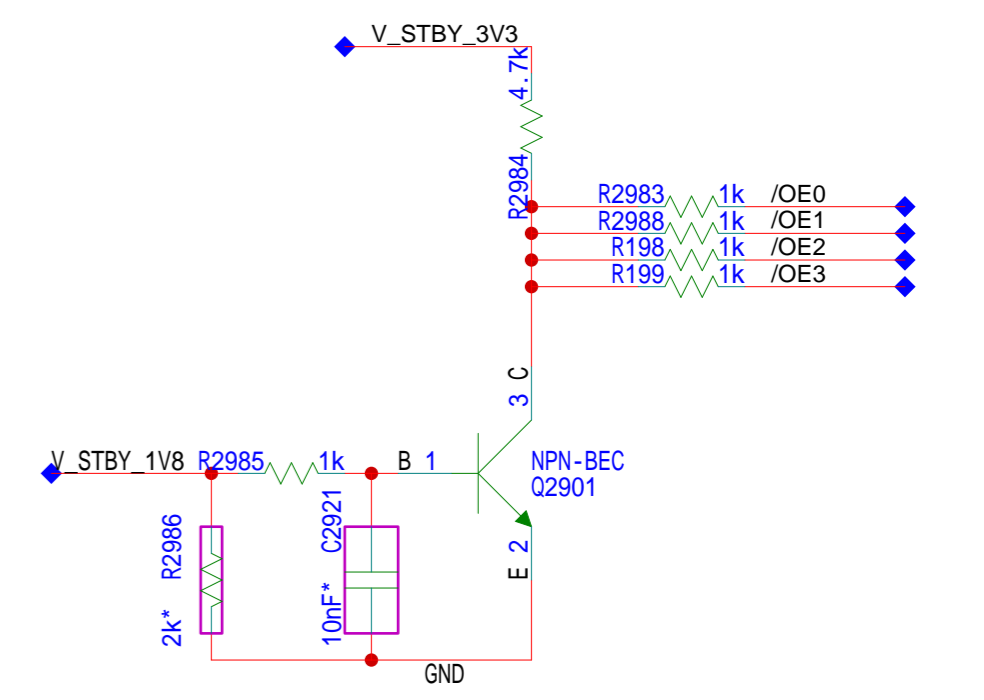
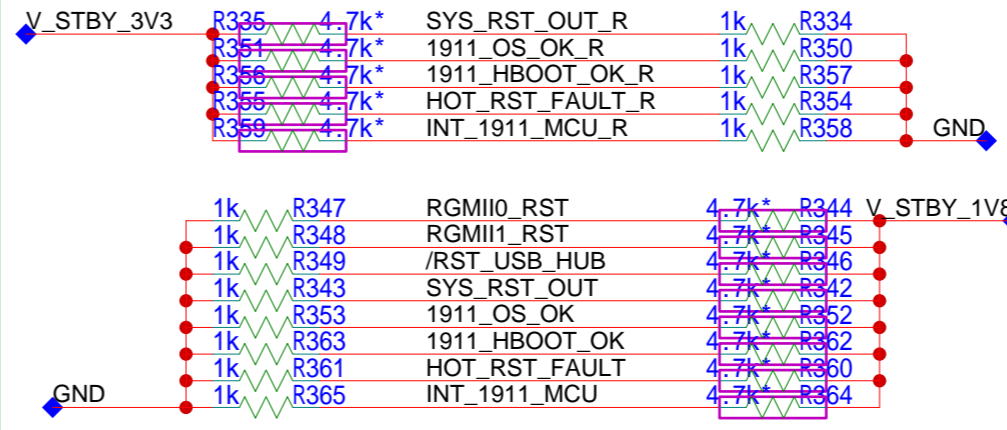
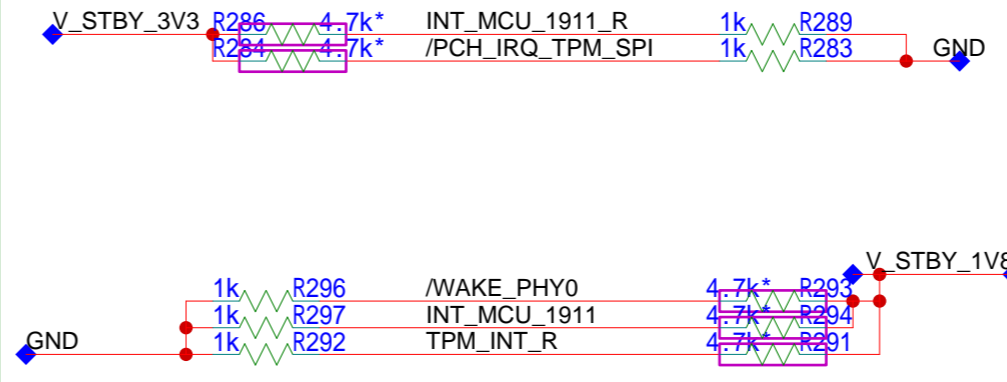
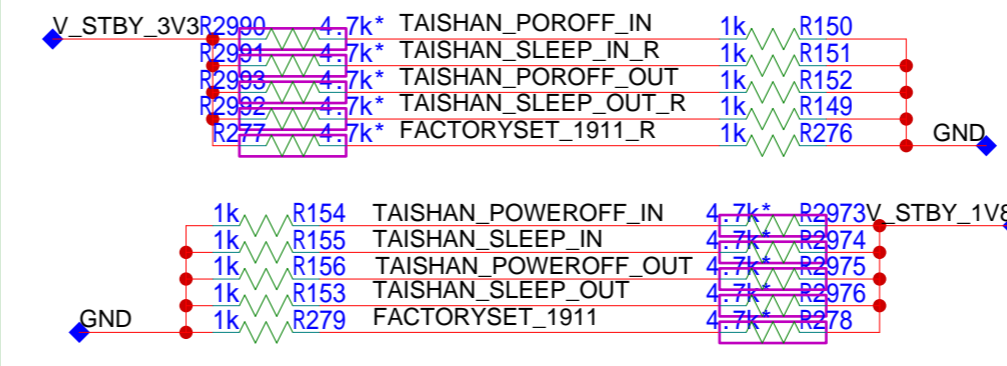
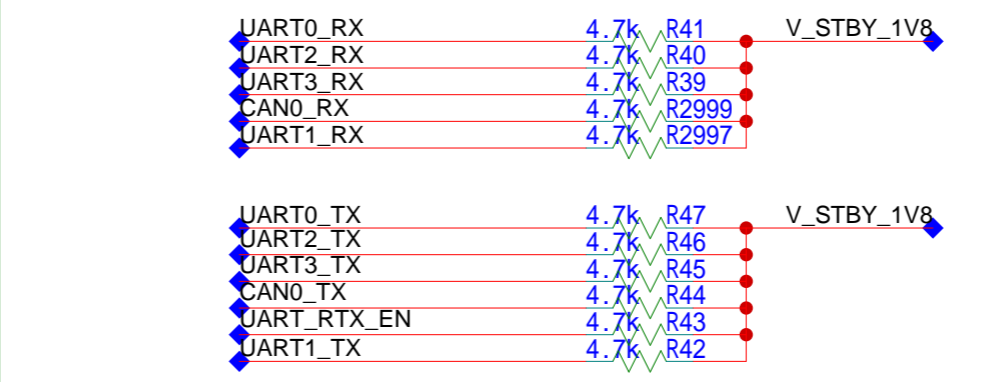
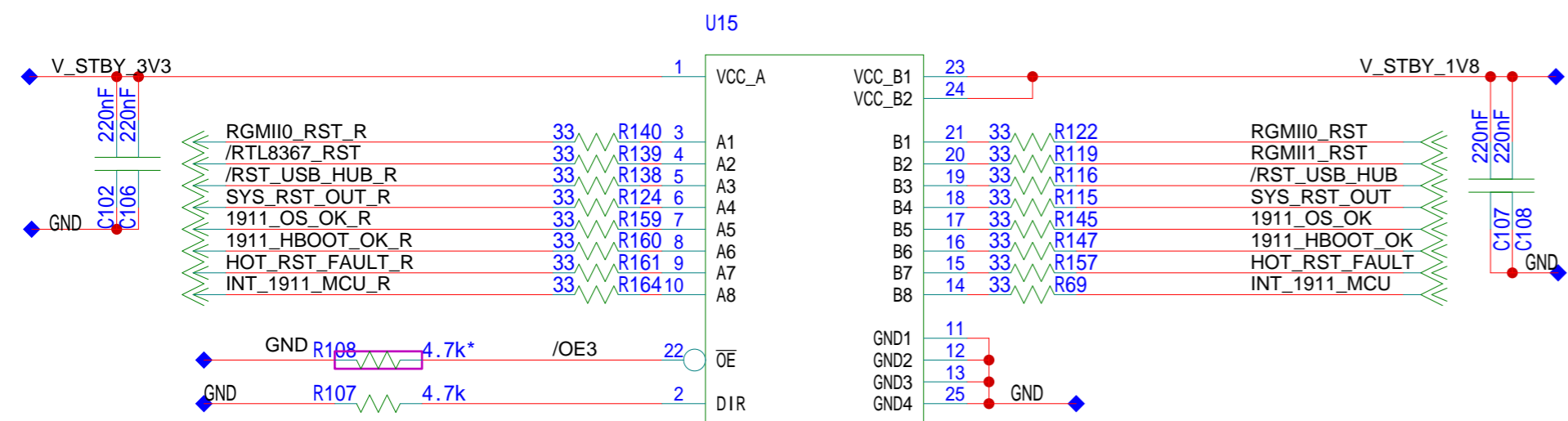
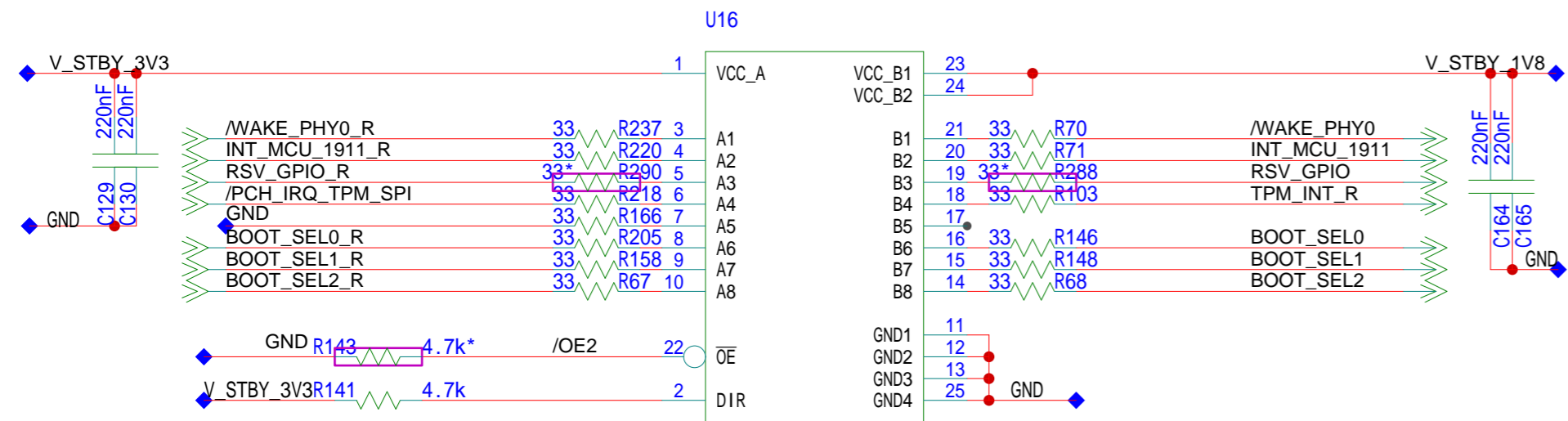
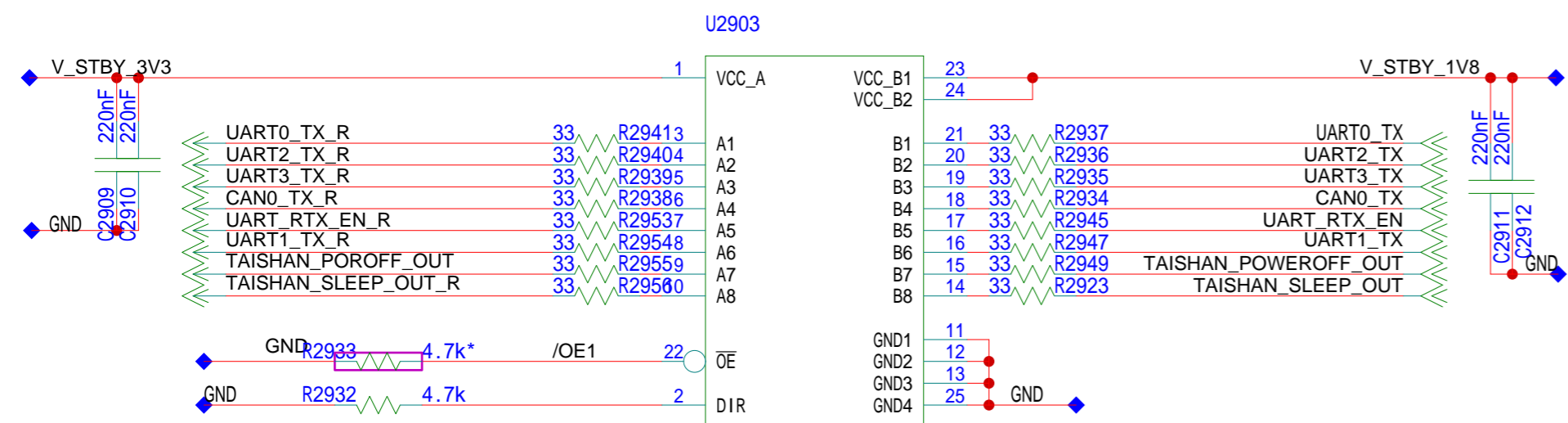
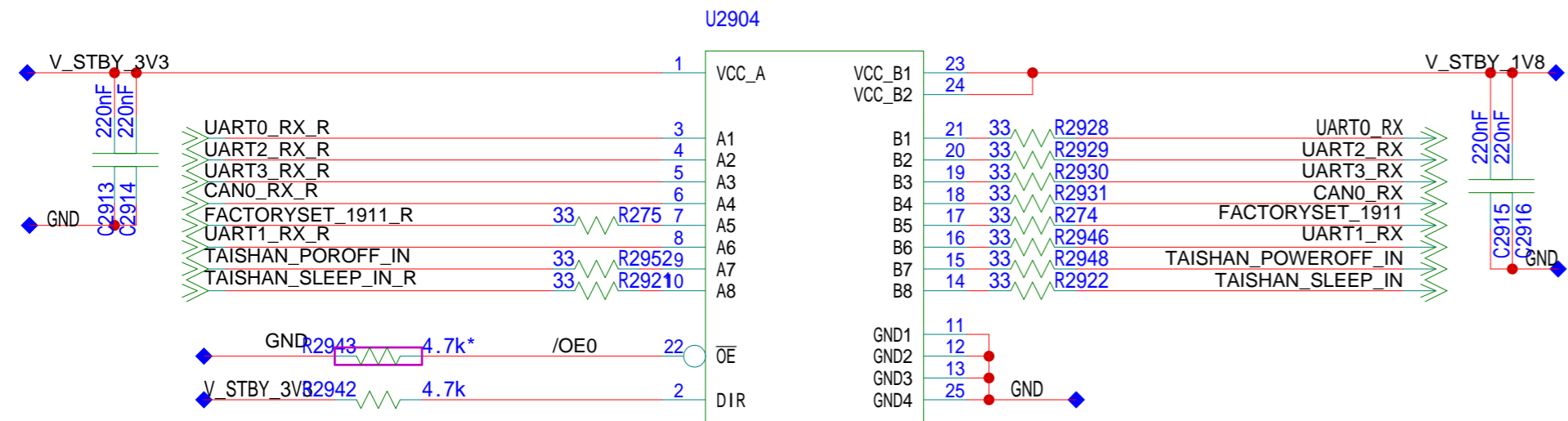
Clock: Crystal



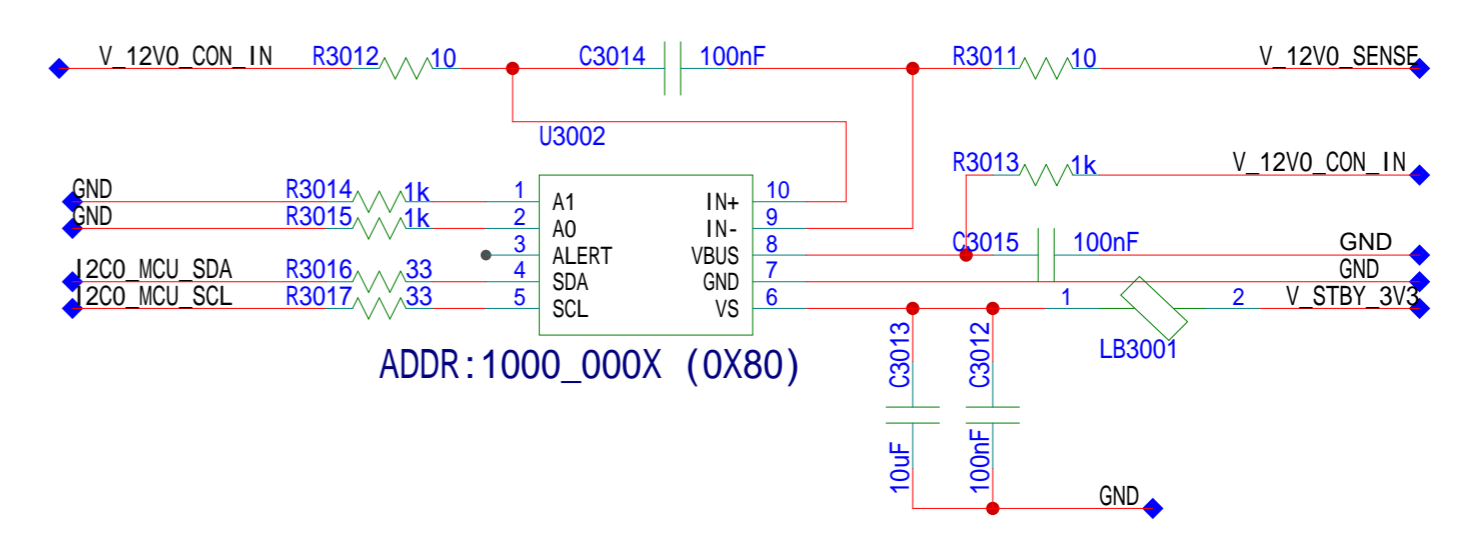
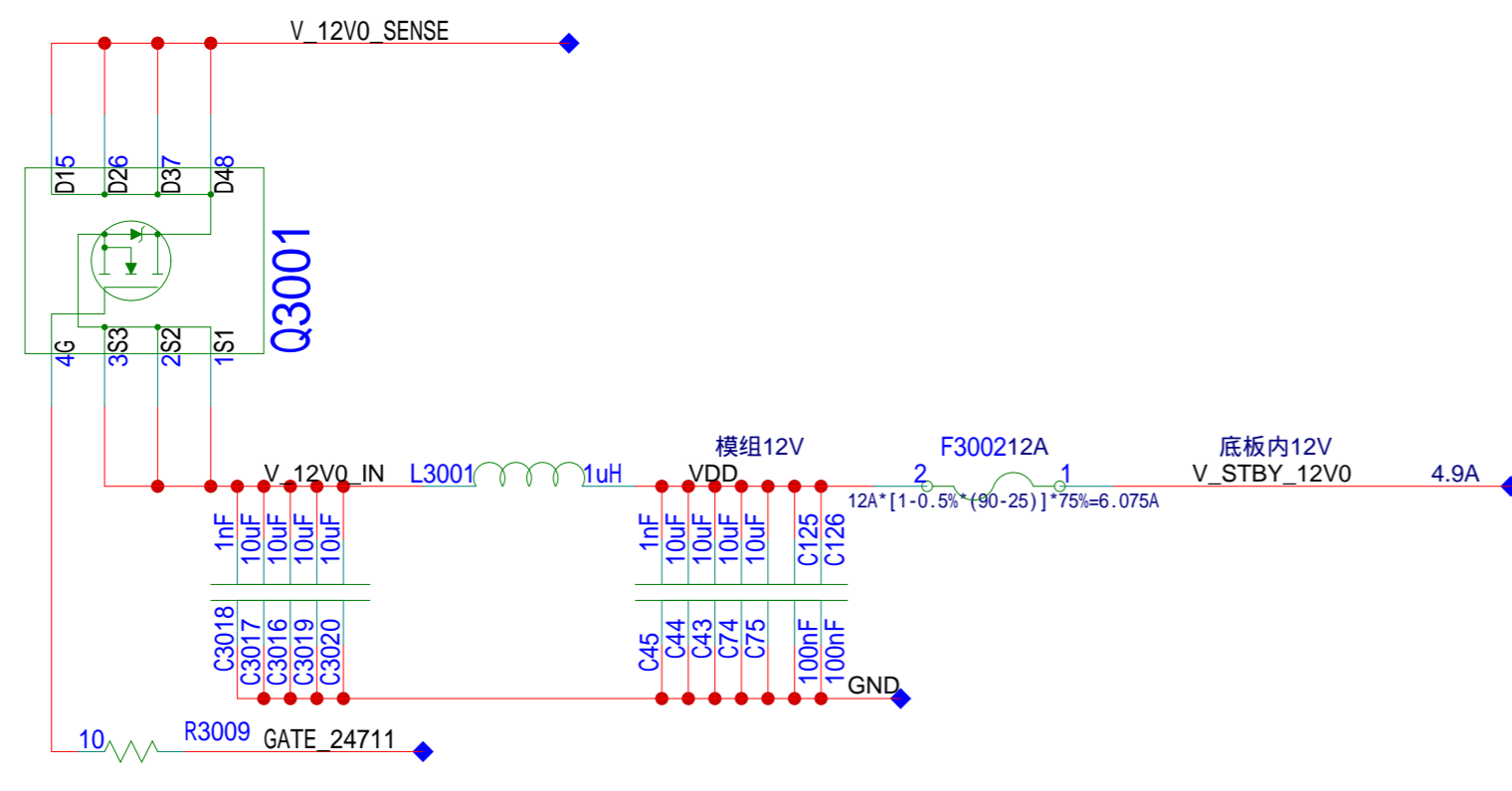
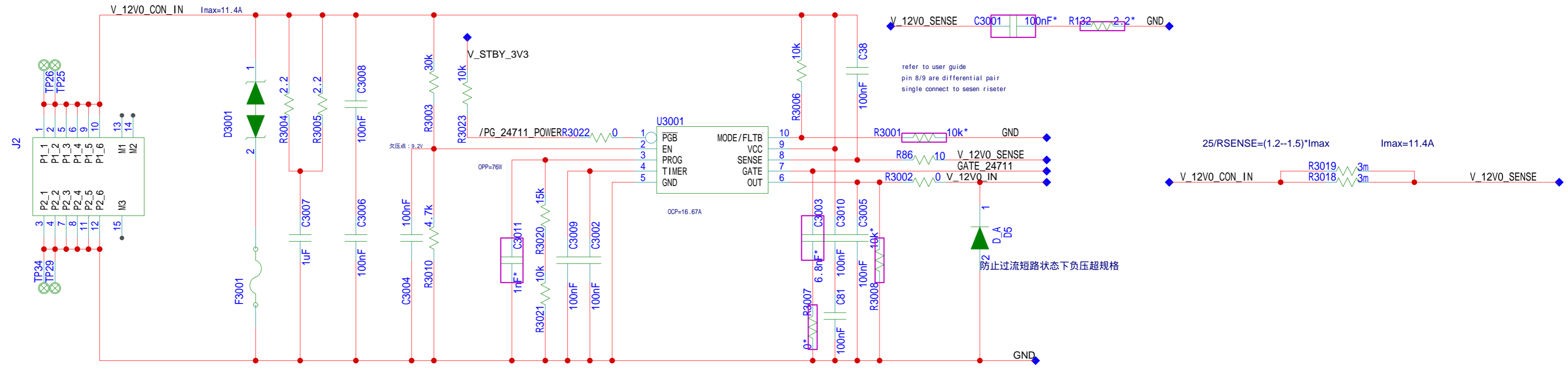
MCU CBB -3



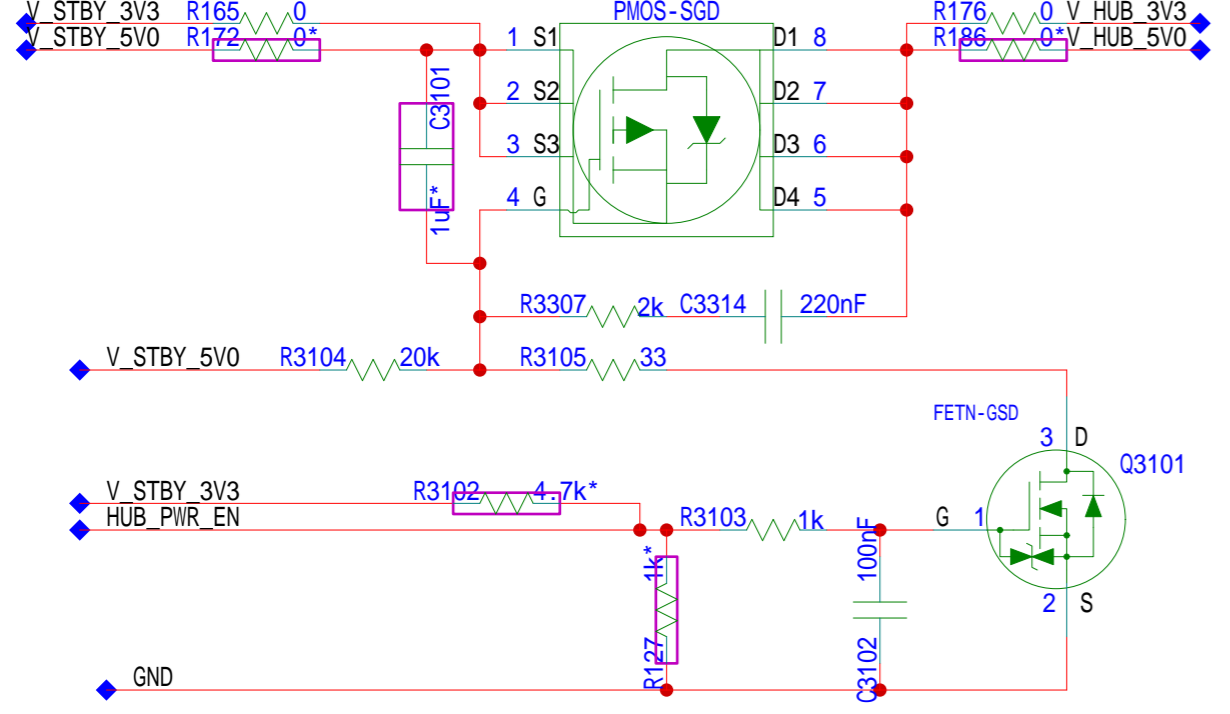
Level Shift



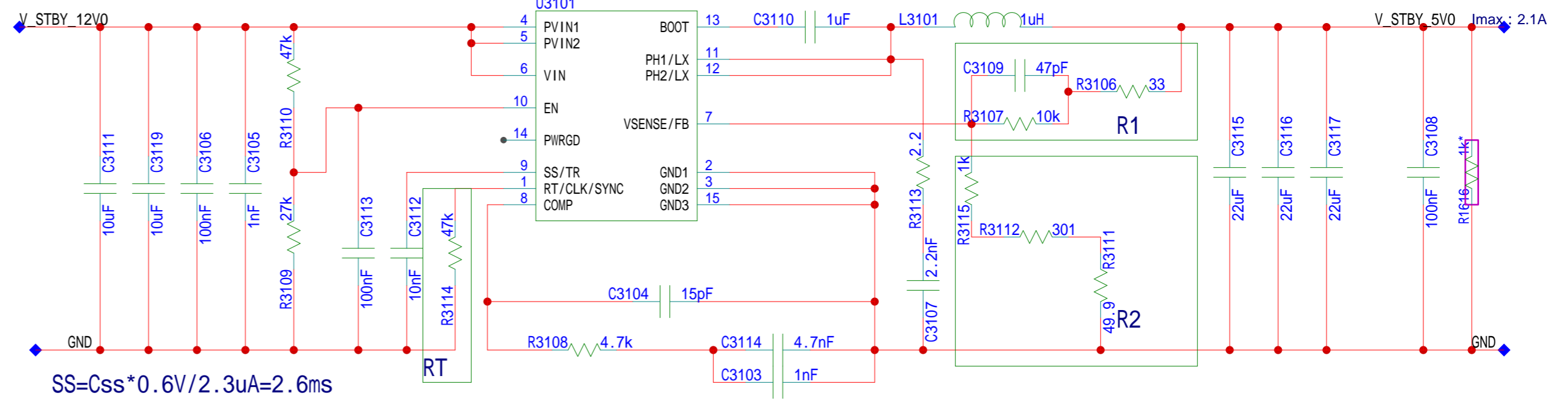
12V Input



Q3102

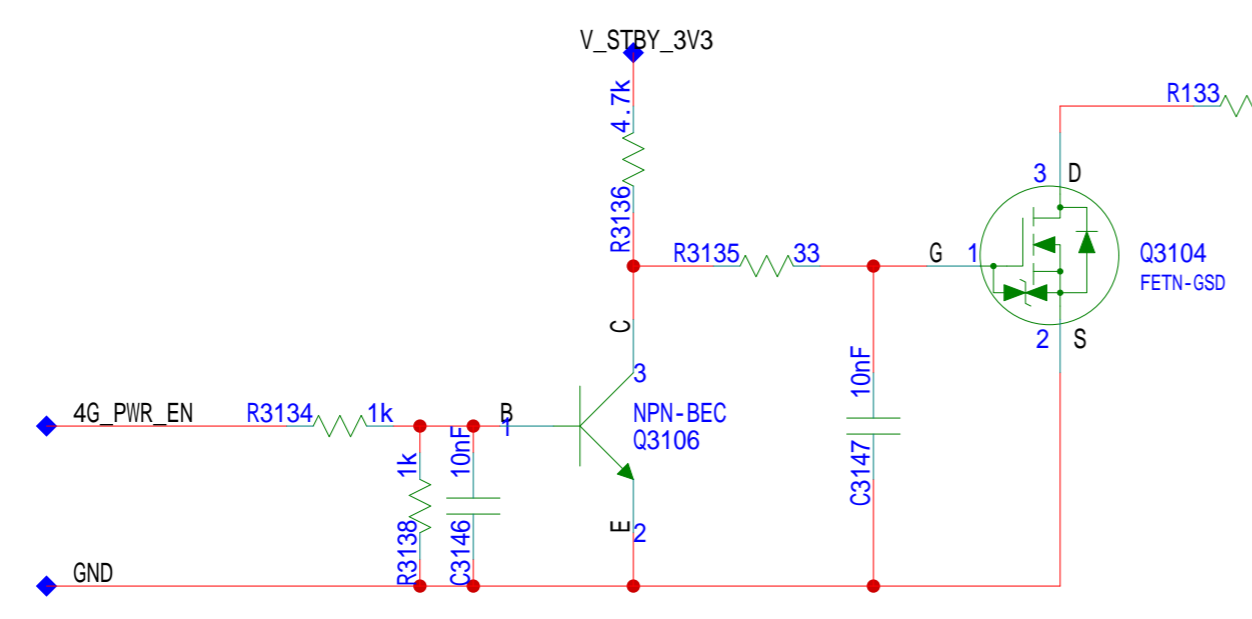


V_12V0 to V_5V0



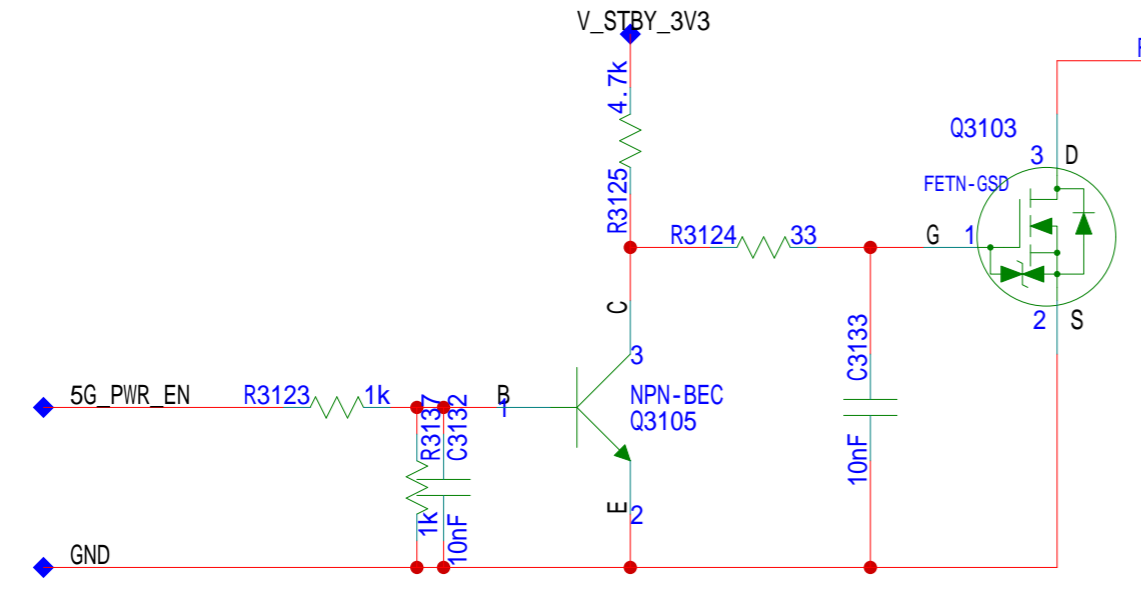
$SS=C_{ss} * 0.6V / 2.3\mu A = 2.6ms$

V_12V0 to V_3V3_LTE



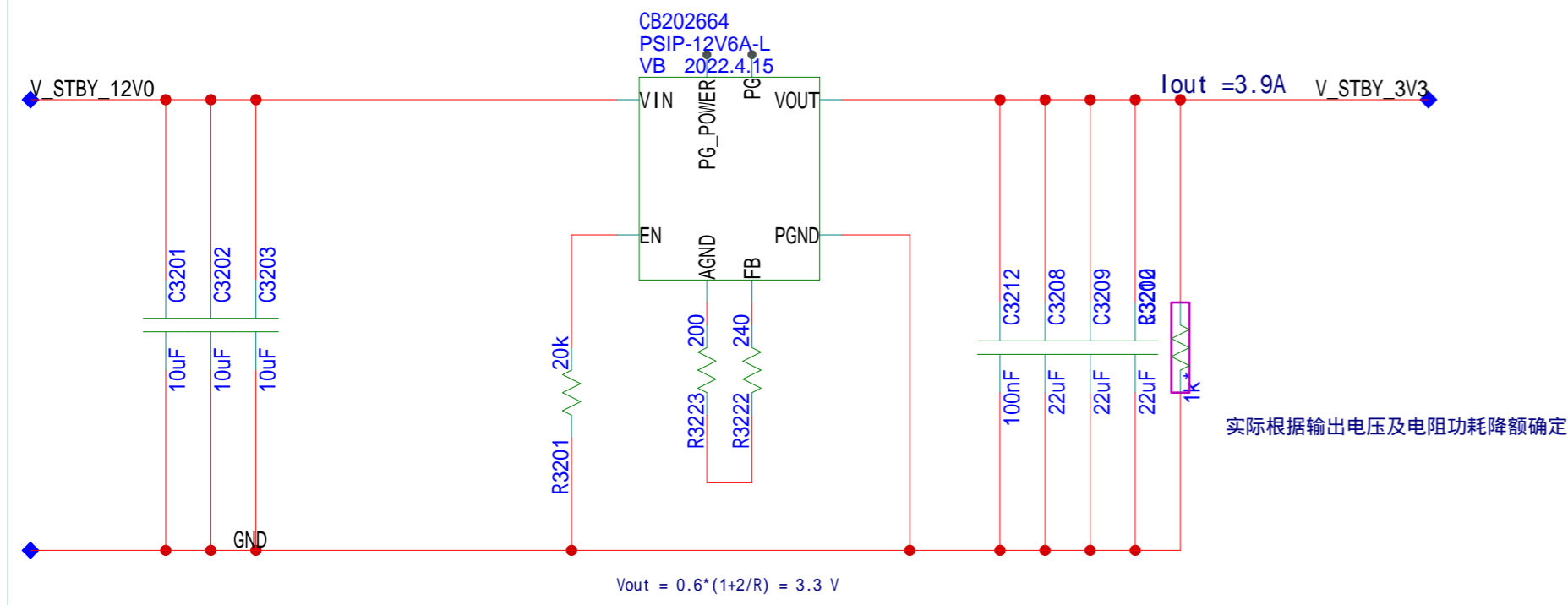
$V_{out}=0.6 * (1+R1/R2)=3.3V$

V_12V0 to V_3V8_LTE

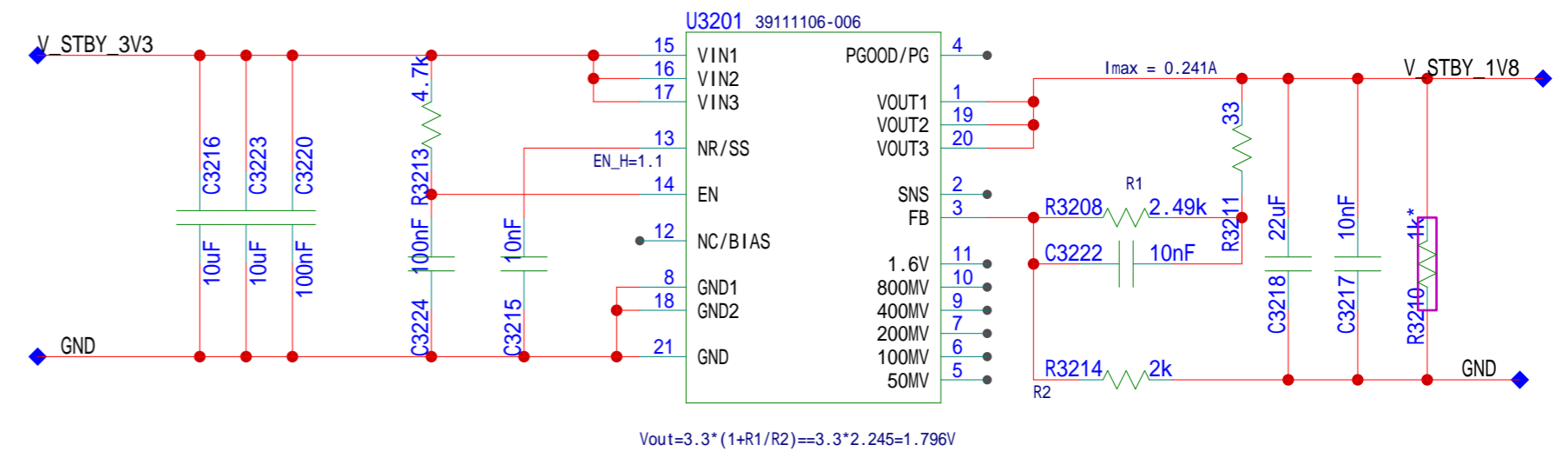


$V_{out}=0.6 * (1+R1/R2)=3.8V$

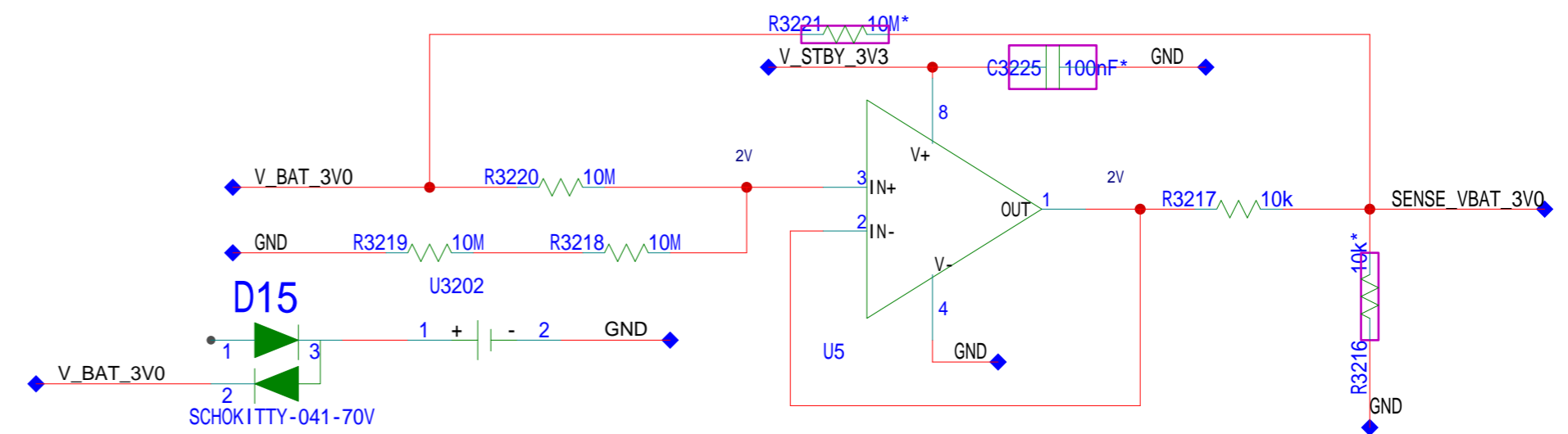
Power 12V to 3V3



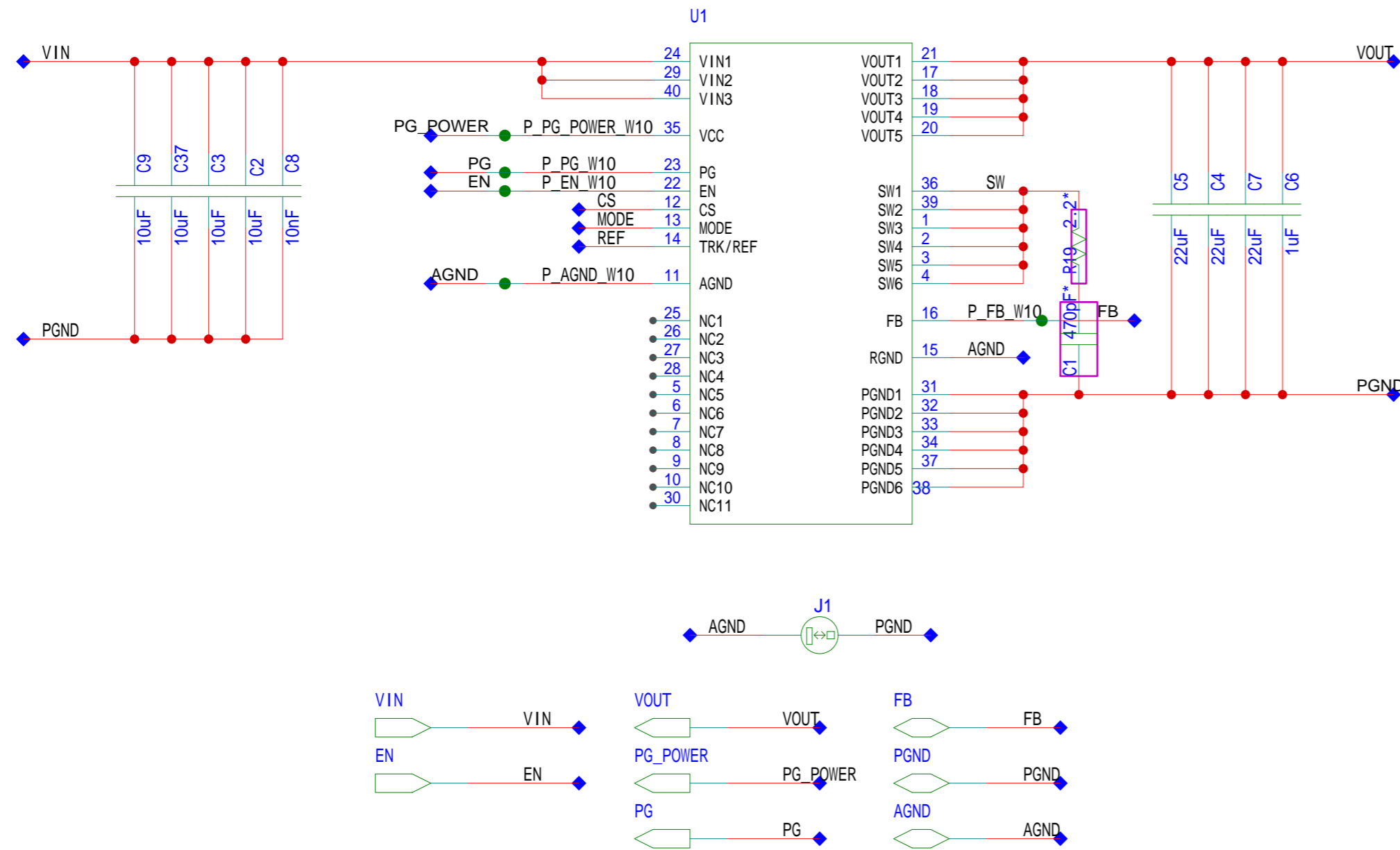
Power 3V3 to 1V8



RTC电源及电压检测



DC-DC CBB

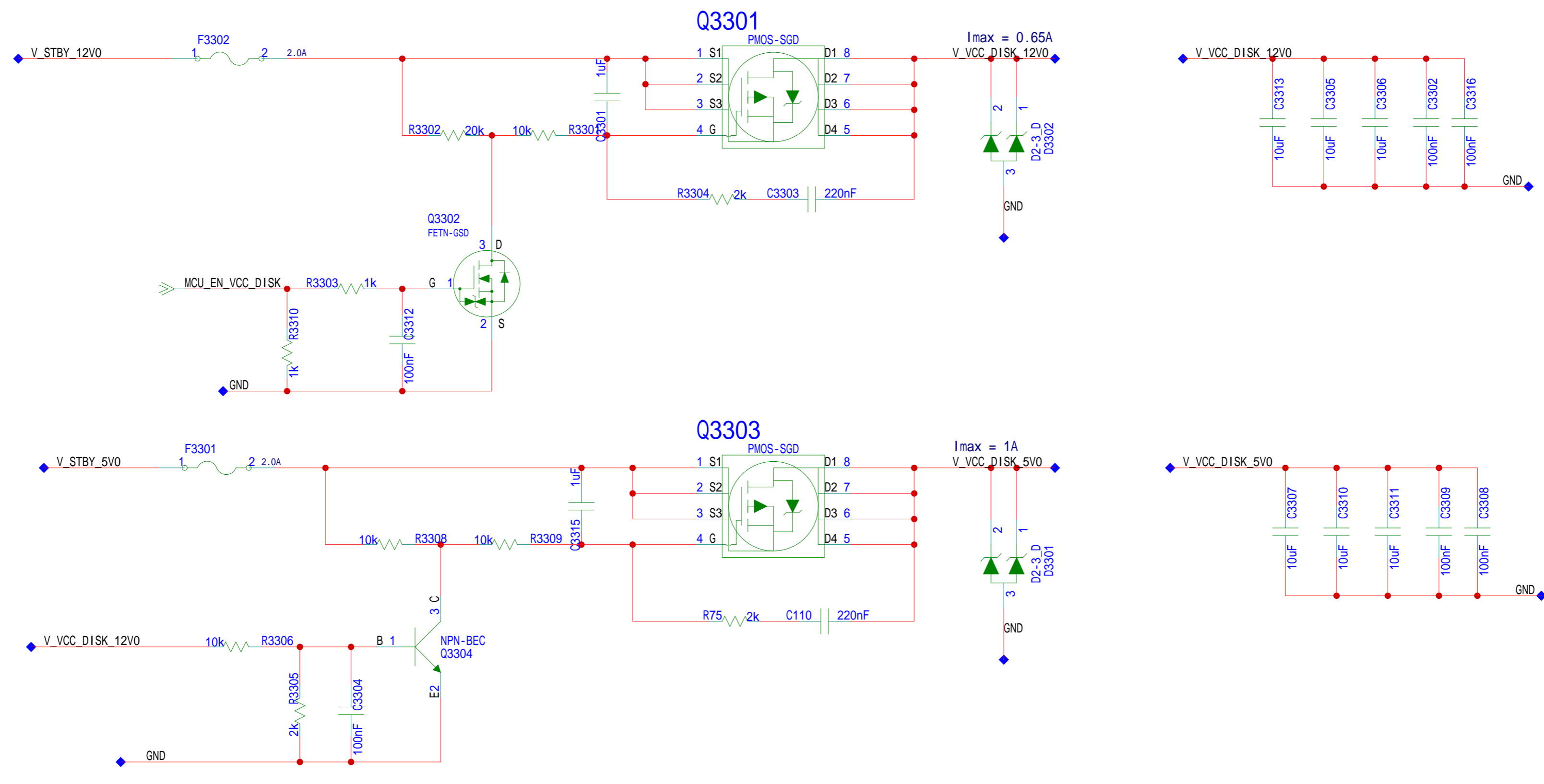


NOTE:详细资料参考应用设计指导书

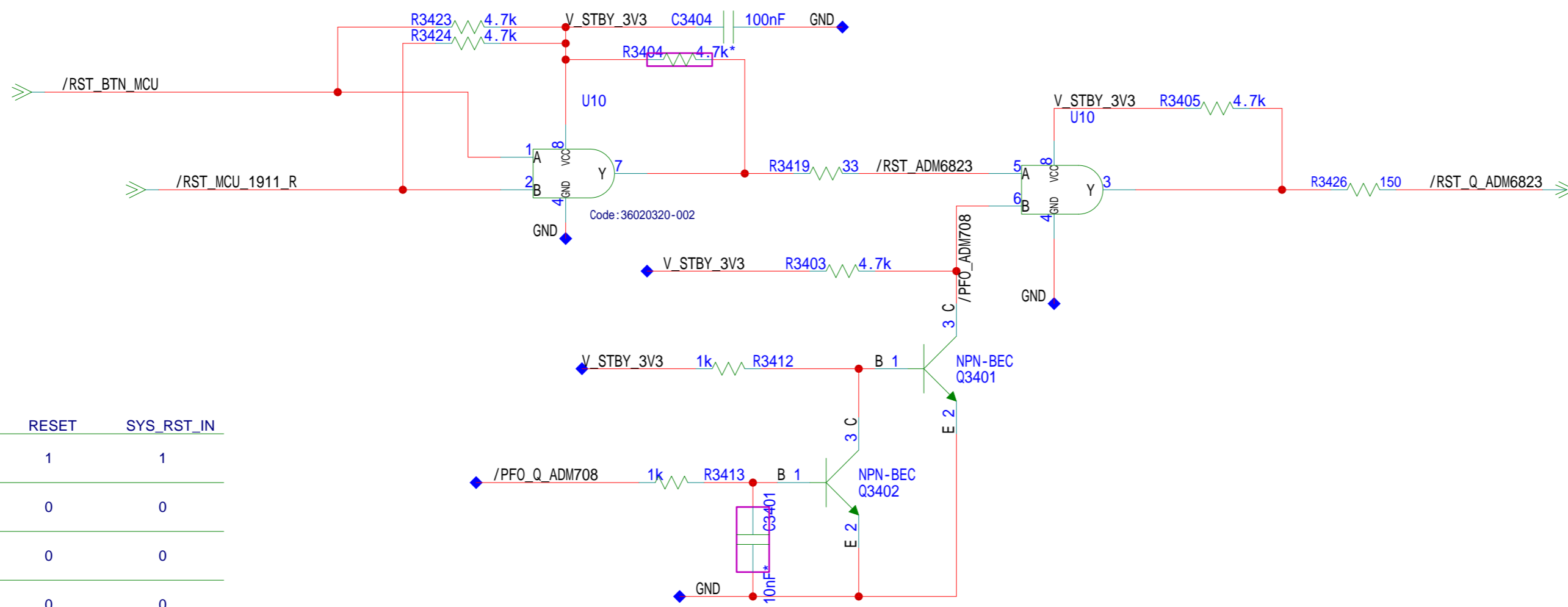
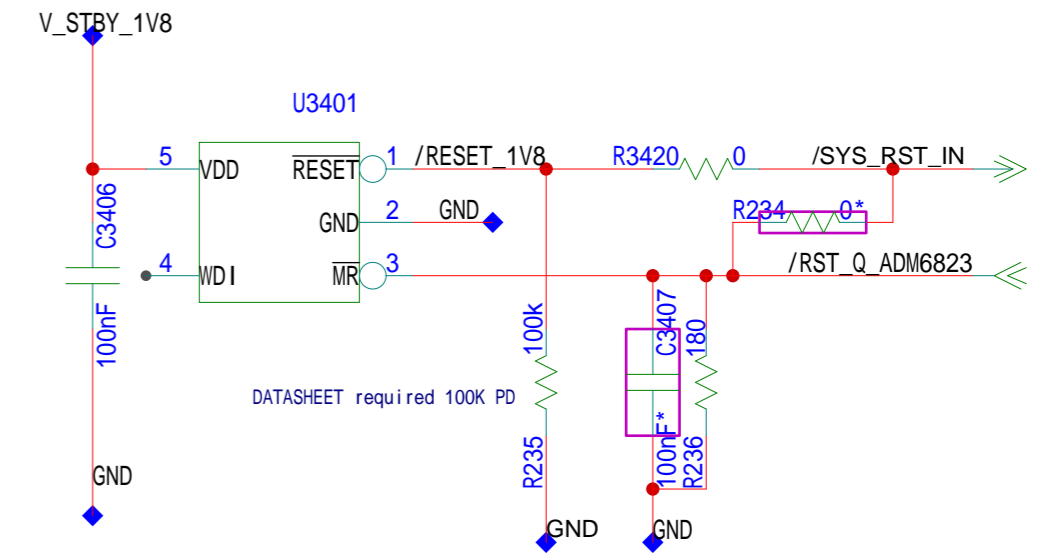
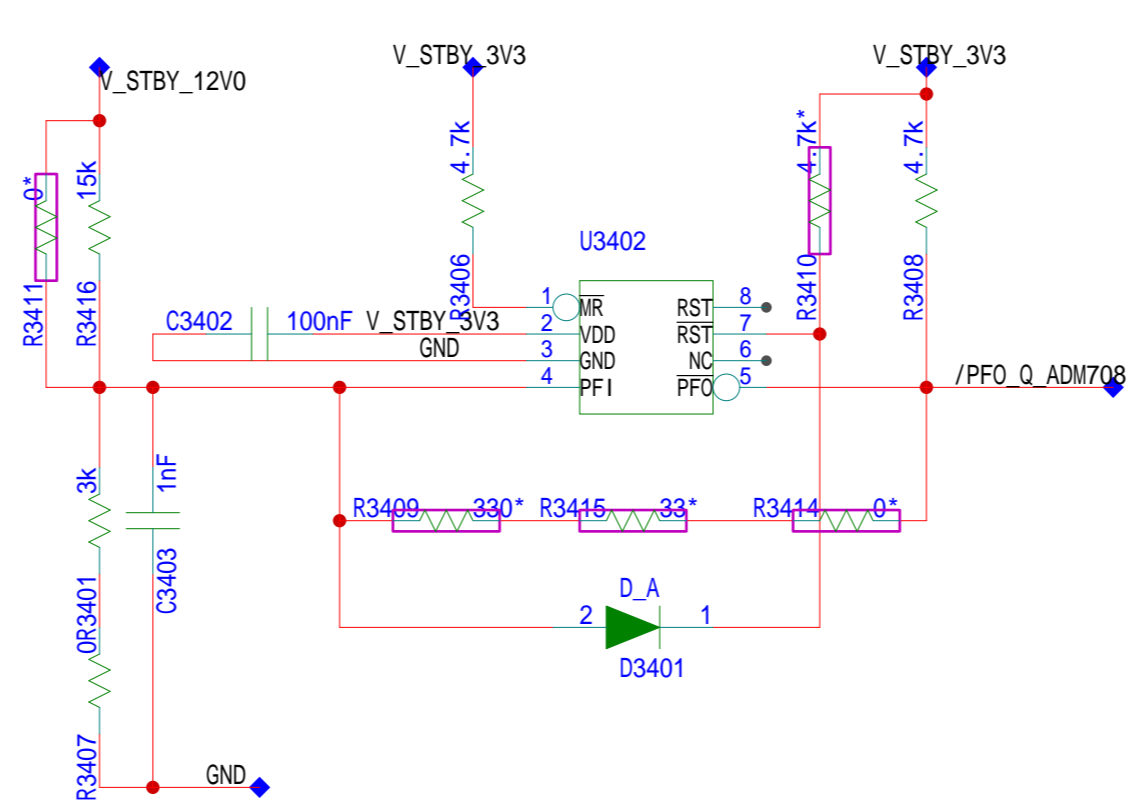
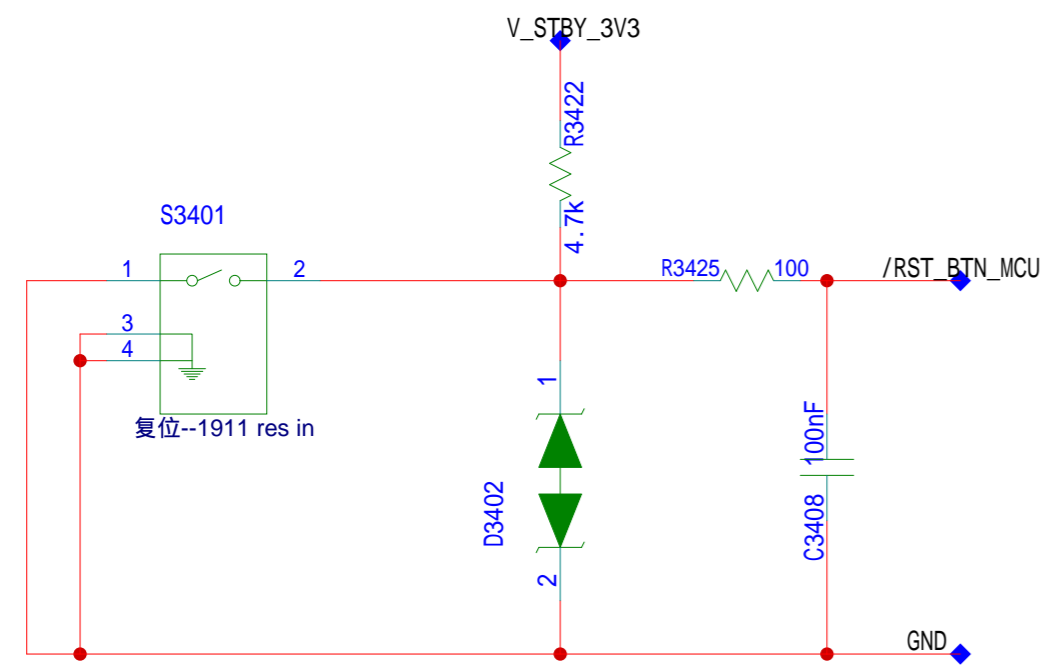
- 1、Vin : Cin最小值为20uF+10nF瓷片电容；
- 2、EN下拉电阻外置；在5V输出及以上场景时，CBB中EN下拉电阻R2001=17.4k（注：如要使用在5V输出以下场景，则需取R2001=20k）；该管脚不要外加电容
- 3、VCC:默认悬空，使用PG时必须上拉到该管脚（3V）
- 4、FB:输出调节，通过FB和RGND之间的电阻来调节输出电压，TRIM调节电阻R1和R2必须选择1%精度电阻。
- 5、PG:不使用PG时悬空，使用时上拉大于等于3K电阻至VCC（3V），且串联一个1K电阻至I/O口，不推荐外部电源（小于3.6V）上拉，外部上拉在EN使能前会有一个0.6V电平；
- 6、MODE:默认悬空，频率设定管脚
- 7、CS:默认悬空，OCP点设定管脚，过流点电阻Rcs（59K）已内置
- 8、Vout : Cout最小值为44uF瓷片电容；
- 9、输出电压与输出电容配置见下表：输出电容选型，请与单板电源工程师讨论

输出电压	0.7V	1.2V	1.8V	3.3V	5.4V
输出电源	9*22UF	7*22UF	5*22UF	4*22UF	3*22UF

SATA Power



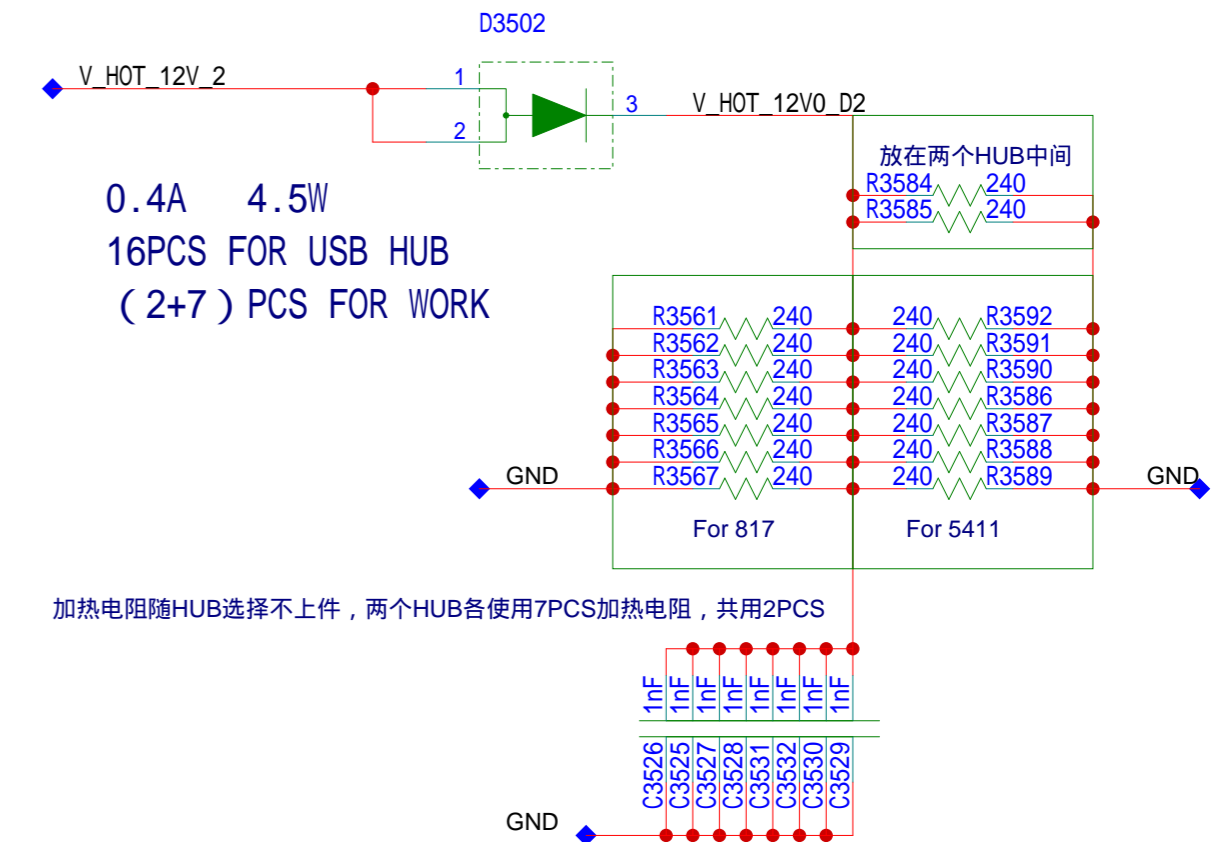
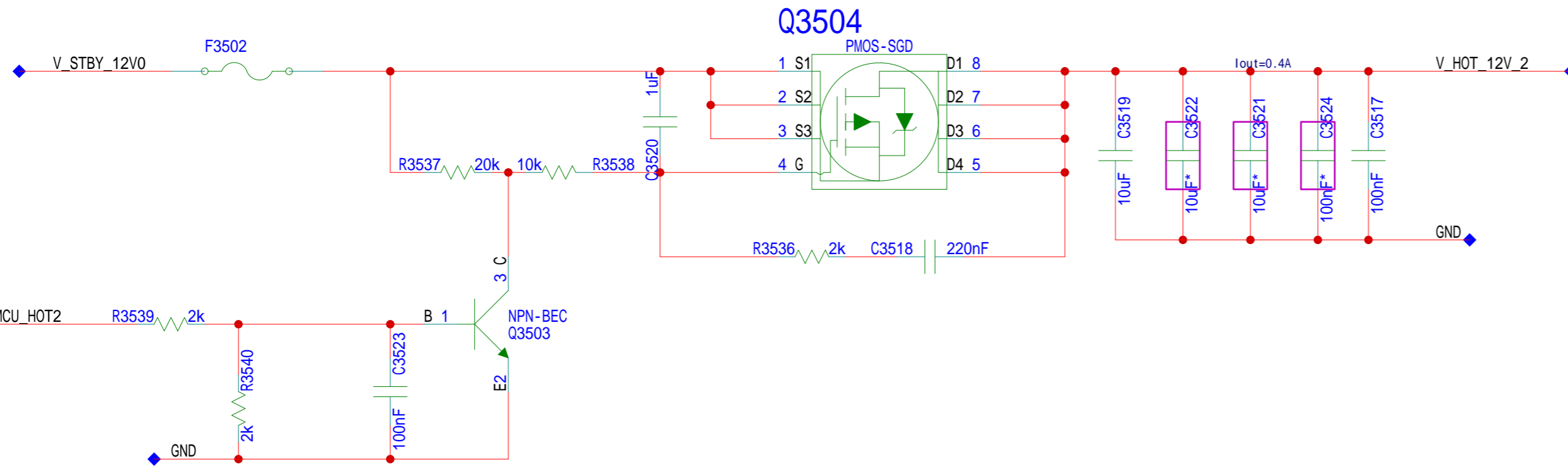
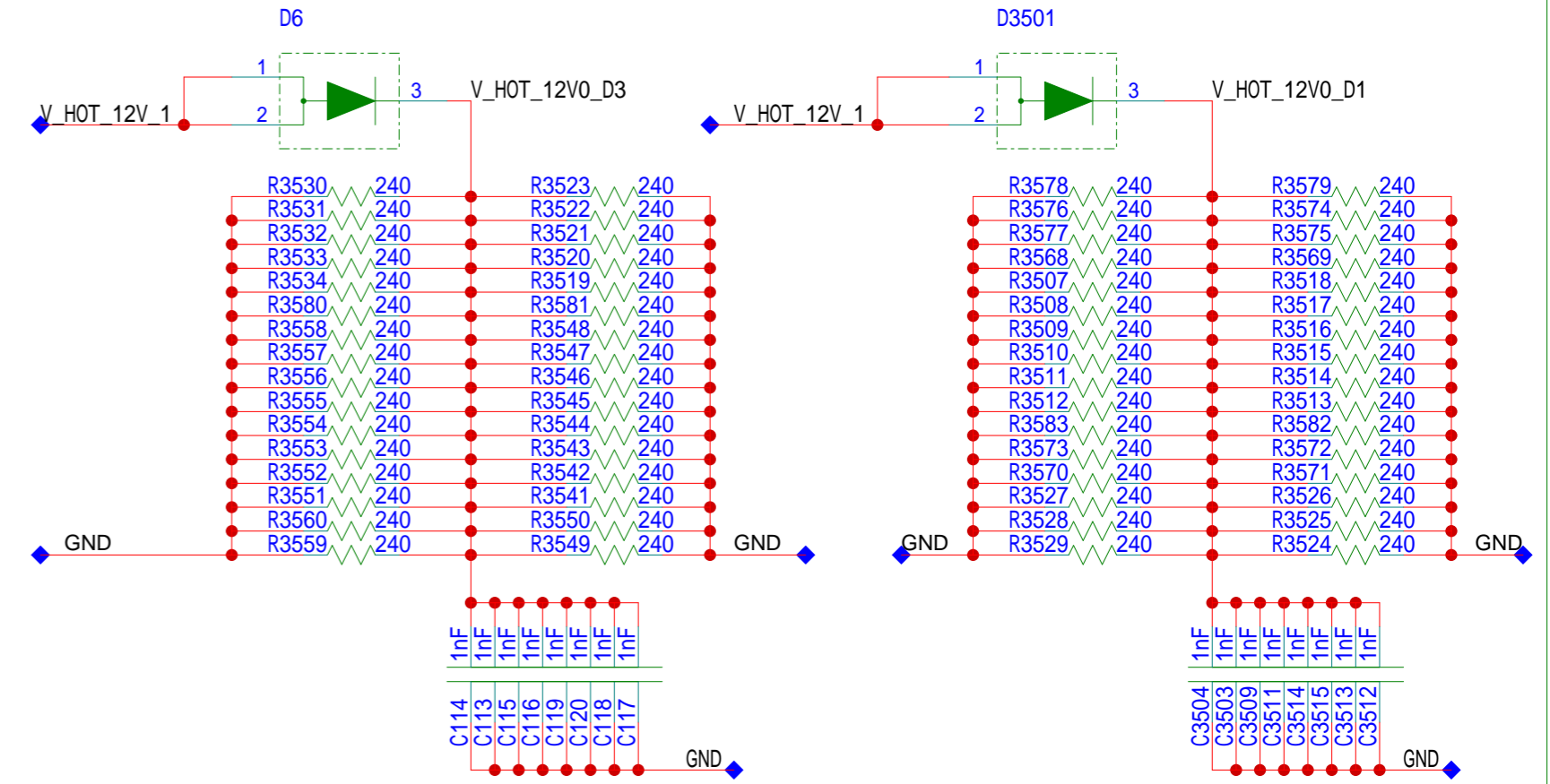
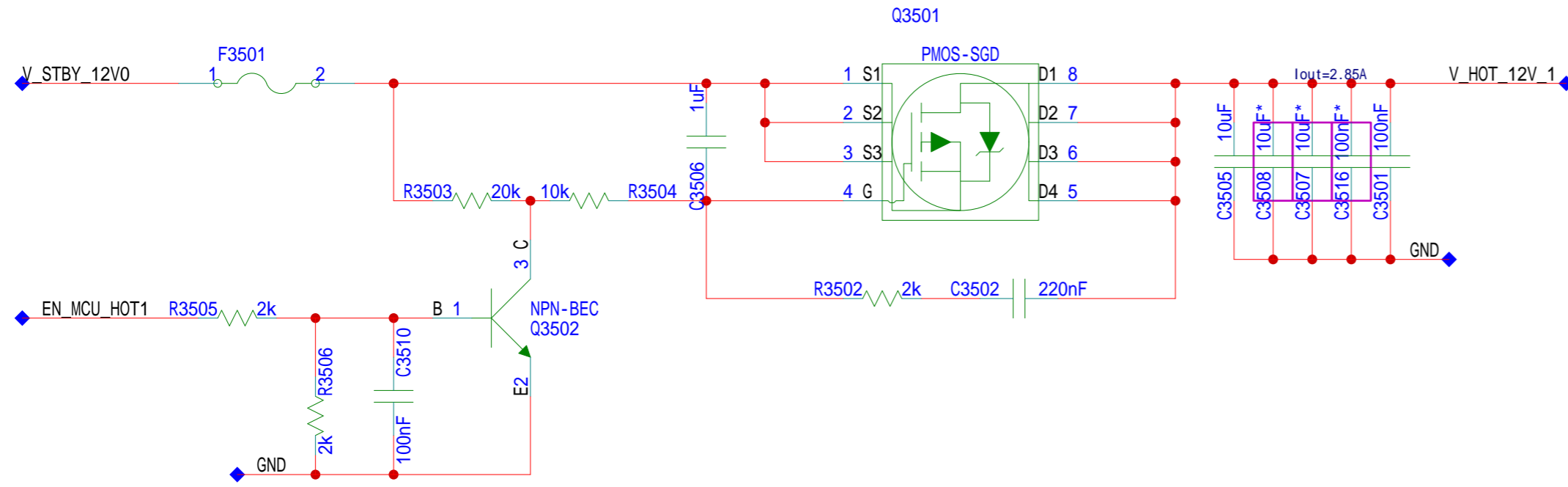
RST BTN



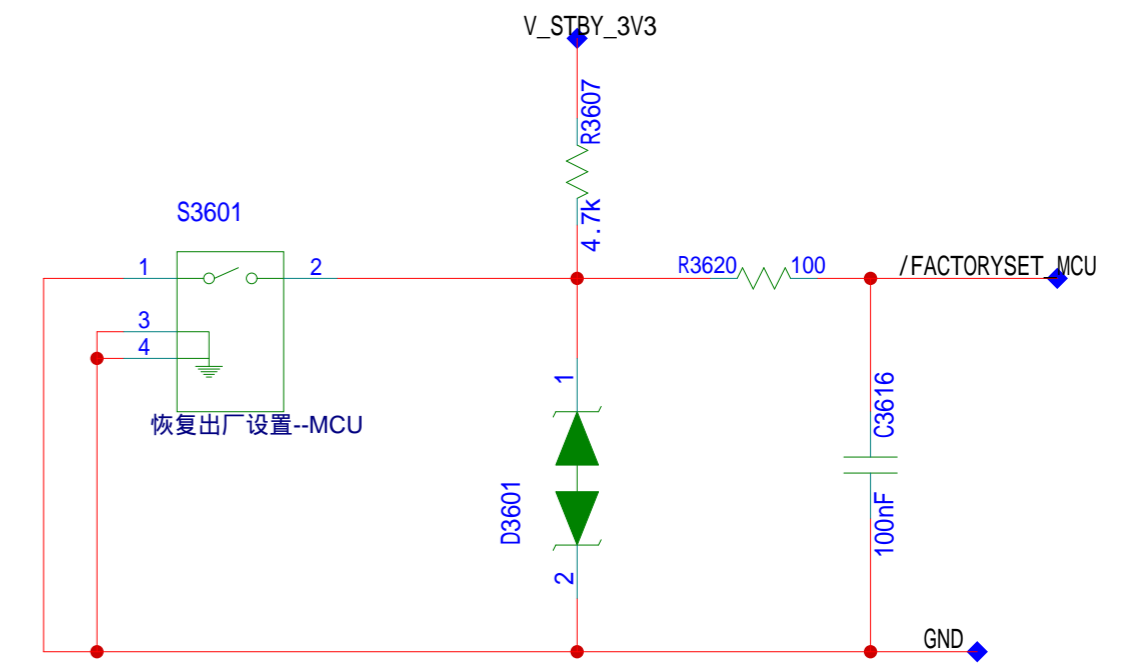
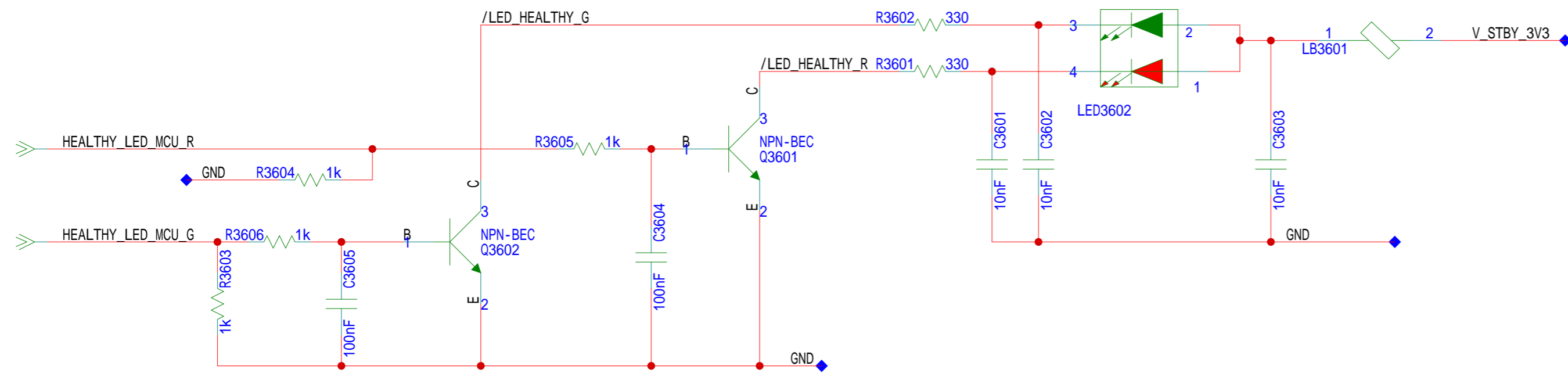
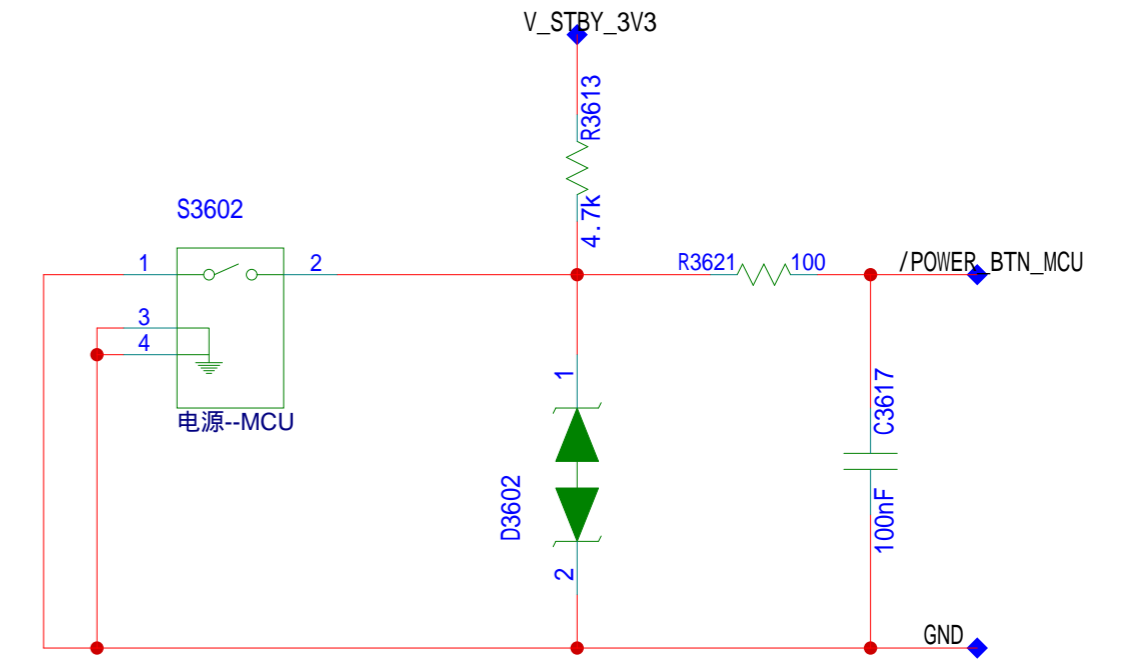
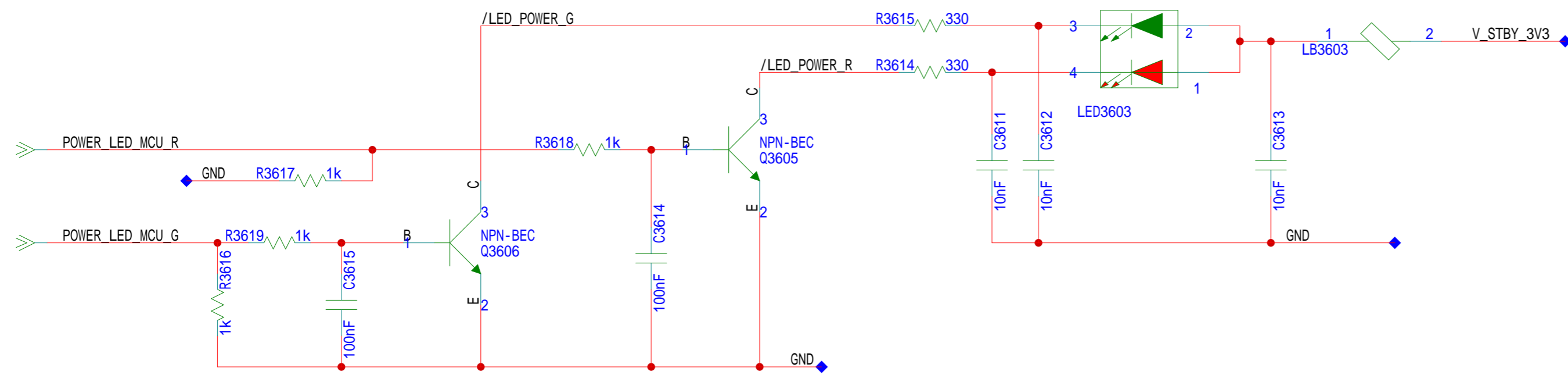
	BTN	MCU	PFO	RESET	SYS_RST_IN
Def	1	1	1	1	1
BTN	0	1	1	0	0
MCU	1	0	1	0	0
PFO	1	1	0	0	0

Heating Resistor

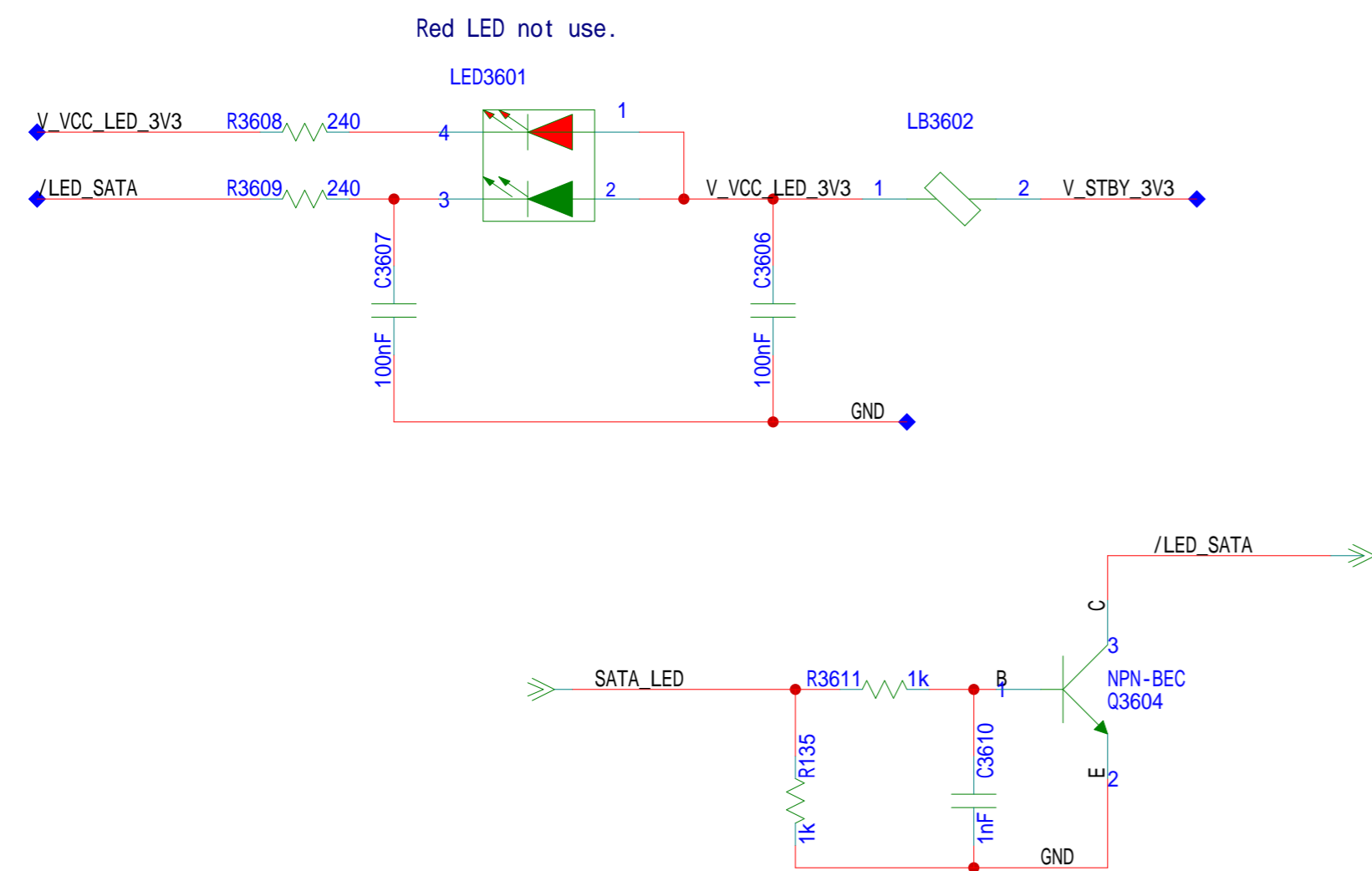
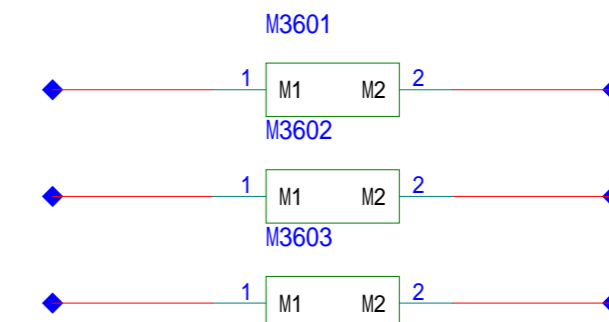
2.85A 32W
64PCS FOR Hi1911



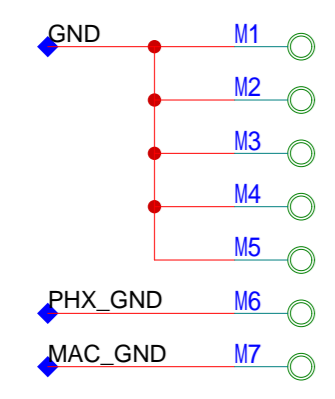
LED & Tact Switch



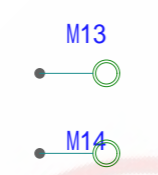
LED导光柱



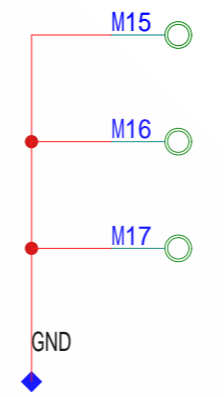
FOR BOARD



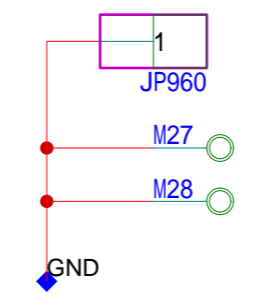
FOR GUIDE PIN



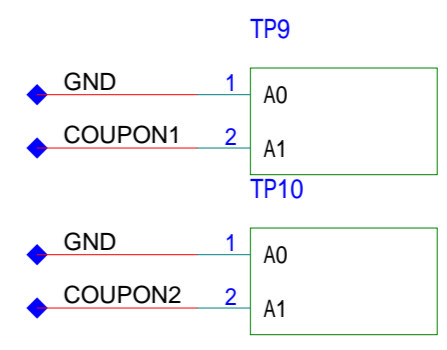
FOR 4G



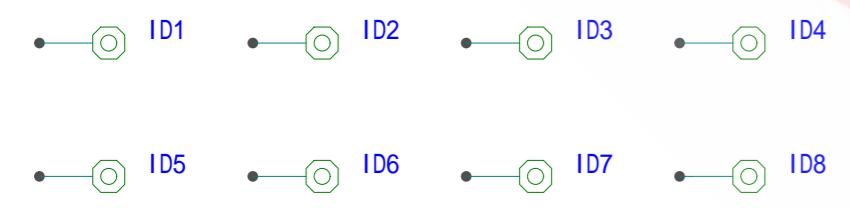
FOR 5G



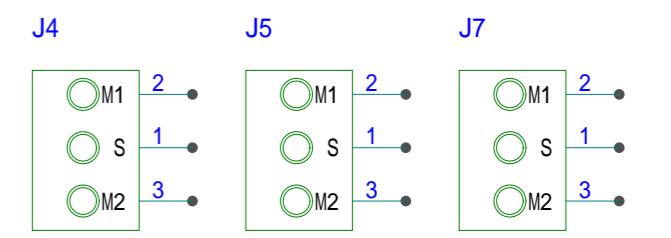
TEST POINT



PCB MARK POINT



FOR MINI BOARD



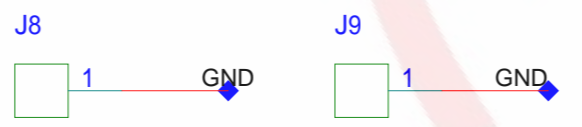
ICT



FOR LTE WIRE



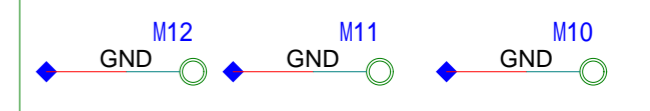
FOR M.2 SSD



FOR MXM



FOR TPM



FOR PHOENIX

